Keysight N6470A Thunderbolt 3 Electrical Compliance Test Application

Methods of Implementation

KEYSIGHT TECHNOLOGIES

Notices

Software Version

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Edition

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Thunderbolt 3 Electrical Compliance Test Application — At A Glance

The Keysight N6470A Thunderbolt 3 Electrical Compliance Test Application allows the testing of all 3rd Generation TBT devices with the Keysight Infiniium Oscilloscope. These tests are based on the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.

The 3rd Generation TBT is defined as an Alternate Mode on the USB Type-C cable and connector infrastructure. It operates with two dual-simplex lanes each running a 10.3125 GB/s, when operating on a passive full featured cable for USB Type-C. The full performance of the 3rd Generation TBT can be enabled when using a Thunderbolt Active Cable and is achieved with two dual-simplex lanes each running at 20.625 GB/s.

The USB Type-C connector in conjunction with a Thunderbolt Controller is capable of providing two dual-simplex lanes (or channels). Each lane provides bi-directional 10.3125 or 20.625 GB/s of bandwidth. The USB Type-C connector is capable of connecting Thunderbolt products when using either a USB Type-C Full Featured cable, a Thunderbolt Passive cable, a Thunderbolt Active Electrical or Optical Cable, or Thunderbolt legacy Cable or Dongle.

The Thunderbolt 3 Electrical Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run, and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE **The tests performed by the Thunderbolt 3 Electrical Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.**

Required Equipment and Software

In order to run the Thunderbolt 3 Electrical Compliance Test Application, you need the following equipment and software:

- N6470A Thunderbolt 3 Electrical Compliance Test Application software.
- The minimum version of Infiniium oscilloscope software (see the N6470A Compliance Test Application release notes).
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Keysight also recommends using a second monitor to view the automated test application.

Table 1 lists the recommended test equipments for running the Thunderbolt Electrical Compliance Tests. Note that all test equipments require calibration to ensure accurate and repeatable results. The test equipments must be calibrated prior to, and if necessary, during the test procedure.

Listed below are the required licenses:

- N6470A Thunderbolt 3 Electrical Compliance Test Application
- Serial Data Analysis (SDA)
- InfiniiScan (SWT)
- EZJIT Plus/EZJIT Complete Software
- Equalization
- InfiniiSim Basic/InfiniiSim Advance

Table 1 Test Equipments and Accessories for Thunderbolt Compliance Tests

Required Equipment	Test Equipment Capabilities/Description	Recommended Test Equipment
Test Point Access Boards	TPA Boards provide test point for the pins on the Thunderbolt connector and an easy way to control the DUT	▪ Thunderbolt Plug Test Fixture or equivalent ▪ Wilder TBT-TPA-UHG2 Thunderbolt Micro-Controller Test Module with USB Cable or equivalent
Real Time Scopes	▪ DC to 21±1GHz -3dB bandwidth or greater ▪ 50G sample/sec Sampling rate or greater, sampling 2 channels simultaneously ▪ Sample memory: 2 channels at 50M samples per channel or greater ▪ 1st and 2nd order CDR capability ▪ Equalization for USB 3.1 model capability	▪ Keysight DSO90000X Series Oscilloscope (25GHz and above)
Pattern Generator	▪ Data rates $\geq$ 20.625 Gbps ▪ Data patterns: PRBS15, PRBS31, Square wave ▪ Differential swing range: 0-2Vp-p in 10mV steps ▪ Rise Time $\geq$ 10 ps (20%-80%) ▪ Intrinsic Jitter $\leq$ 400 fS RMS	▪ Keysight JBERT M8000 series - High performance BERT, Configuration for Bench-Top 5-Slot Chassis ▪ M8020A-BU2 (AXIe chassis, 5-slot) ▪ M8041A-G16 (Pattern Generator one channel, data rate up to 16 Gbps) ▪ M8041A-0G2 (Second Channel for pattern generator, license) ▪ M8041A-0G3 (Advanced jitter sources for receiver characterization, module wide license) ▪ M8062A-G32 (32 Gbps Pattern generator front end) ▪ M8062A-0G4 (Multi-tap De-emphasis license) ▪ M8070A-0TP (Transportable License for M8000 Software)
Network Analyzer	▪ 2 ports used simultaneously ▪ At least 1 MHz - 13 GHz bandwidth ▪ Dynamic Range > 50 dB	▪ Keysight E5071C ENA Series Network Analyzer
Signal Generator	▪ Frequency range of at least 10-400 MHz ▪ Output power of ±15dBm	▪ Holzworth HS1001C
Accessories		
Low insertion loss phase matched cables	▪ Phase matched ±2° @ 40GHz ▪ Max IL in 10GHz < 1.2dB	▪ Rosenberger UK Micro Coax FC142A0-014-MTIE 2.92m (x2) L-1m (40GHz) ▪ Rosenberger Adaptor: RPC-2.92 female – SMP female - 02K119-K00E3
ISI Channel	▪ Varied insertion loss of 2-10dB @5GHz and @10GHz	▪ BertScope differential ISI board
Pick Off Tee	▪ Pick off tees with bandwidth of at least 40GHz	▪ 2 x Picosecond Tek PSPL5361 Pickoff Tee
Splitter	▪ Splitter with bandwidth of at least 1GHz	▪ 1 x Mini Circuits ZFSC-2-2-S+
DC Block	▪ DC Blocks with bandwidth of at least 33GHz ▪ 1 dB Insertion Loss to 40 GHz ▪ Capacitance of at least 0.22 µF	▪ 2 x Picosecond Tek PSPL5509 DC Block

In This Book

This manual describes the tests that are performed by the Thunderbolt 3 Electrical Compliance Test Application in more detail.

- Chapter 1, “Installing the Thunderbolt 3 Electrical Compliance Test Application” describes how to install and license the Thunderbolt Electrical Compliance Test Application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” describes how to start the Thunderbolt 3 Electrical Compliance Test Application and gives a brief overview of its features.
- Chapter 3, “Host / Device Thunderbolt 3 Transmitter Testing” contains an overview on the Thunderbolt system components and requirements for Transmitter testing.
- Chapter 4, “Transmitter Tests for 10.3125 GB/s Systems” describes procedures to run electrical tests on a Thunderbolt DUT operating at a bit rate of 10.3125 GB/s.
- Chapter 5, “Transmitter Tests for 20.625 GB/s Systems” describes procedures to run electrical tests on a Thunderbolt DUT operating at a bit rate of 20.625 GB/s.
- Chapter 6, “Calibrating the Infiniium Oscilloscope” describes how to calibrate the oscilloscope in preparation for running the Thunderbolt compliance tests.
- Chapter 7, “InfiniiMax Probing” describes the probe amplifier and probe head recommendations for Thunderbolt compliance testing.

See Also

- The Thunderbolt 3 Electrical Compliance Test Application’s Online Help, which describes:
  - Starting the Thunderbolt Compliance Test Application.
  - Creating or opening a test project.
  - Setting up the Thunderbolt test environment.
  - Selecting tests.
  - Configuring selected tests.
  - Defining compliance limits.
  - Connecting the oscilloscope to the DUT.
  - Running tests.
  - Automating the application.
  - Viewing test results.
  - Viewing/exporting/printing the HTML test report.
  - Saving test projects.
  - Installing/removing add-ins.
  - Controlling the application via a remote PC.
  - Using a second monitor.
- The Thunderbolt standard specifications are available in *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5* and *Thunderbolt Interconnect Specification Rev 1.5*.

Contents

1 Installing the Thunderbolt 3 Electrical Compliance Test Application

If you purchased the N6470A Thunderbolt 3 Electrical Compliance Test Application separately, you must install the software and license key.

Installing the Software

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see the N6470A test application release notes) by choosing **Help>About Infiniium**... from the main menu.
2. To obtain the Thunderbolt 3 Electrical Compliance Test Application, go to Keysight Web site: http://www.keysight.com/find/scope-apps-sw/.
3. The link for Thunderbolt 3 Electrical Compliance Test Application will appear. Double-click the link and follow the instructions to download and install the application software.

Installing the License Key

1 Request a license code from Keysight by following the instructions on the Entitlement Certificate.
You will need the Oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium**... dialog box.
2 After you receive your license code from Keysight, choose **Utilities>Install Legacy Licenses...**.
3 In the Install Option License dialog, enter your license code and click **Install License**.
4 Click **OK i**n the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.
5 Click **Close** to close the Install Option License dialog.
6 Choose **File>Exit**.
7 Restart the Infiniium oscilloscope application software to complete the license installation.

2 Preparing to Take Measurements

Before running the Thunderbolt 3 Electrical Compliance tests, you must calibrate the oscilloscope and probe. After the oscilloscope and probe have been calibrated, you are ready to start the Thunderbolt 3 Electrical Compliance Test Application and perform the measurements. Additionally, some of the tests require Preset Calibration and CTLE Calibration before running the respective tests.

Calibrating the Oscilloscope

- If you have not already calibrated the oscilloscope and probe, see Chapter 6, “Calibrating the Infiniium Oscilloscope”.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities>Calibration** menu.

NOTE If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the Thunderbolt 3 Electrical Compliance Test Application

1 From the Infiniium Oscilloscope's main menu, choose **Analyze>Automated Test Apps>N6470A Thunderbolt Test App.**

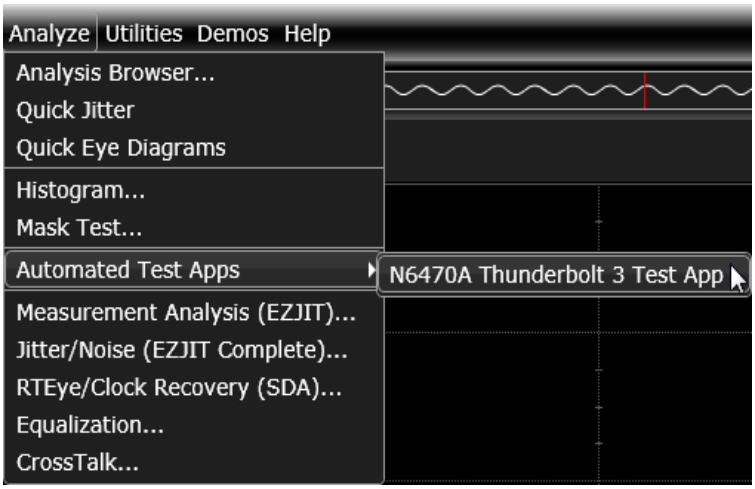


Figure 1 Starting the Thunderbolt Electrical Compliance Test Application

NOTE

If the N6470A Thunderbolt Test App does not appear in the **Automated Test Apps** menu, the Thunderbolt 3 Electrical Compliance Test Application has not been installed (see Chapter 1, "Installing the Thunderbolt 3 Electrical Compliance Test Application").

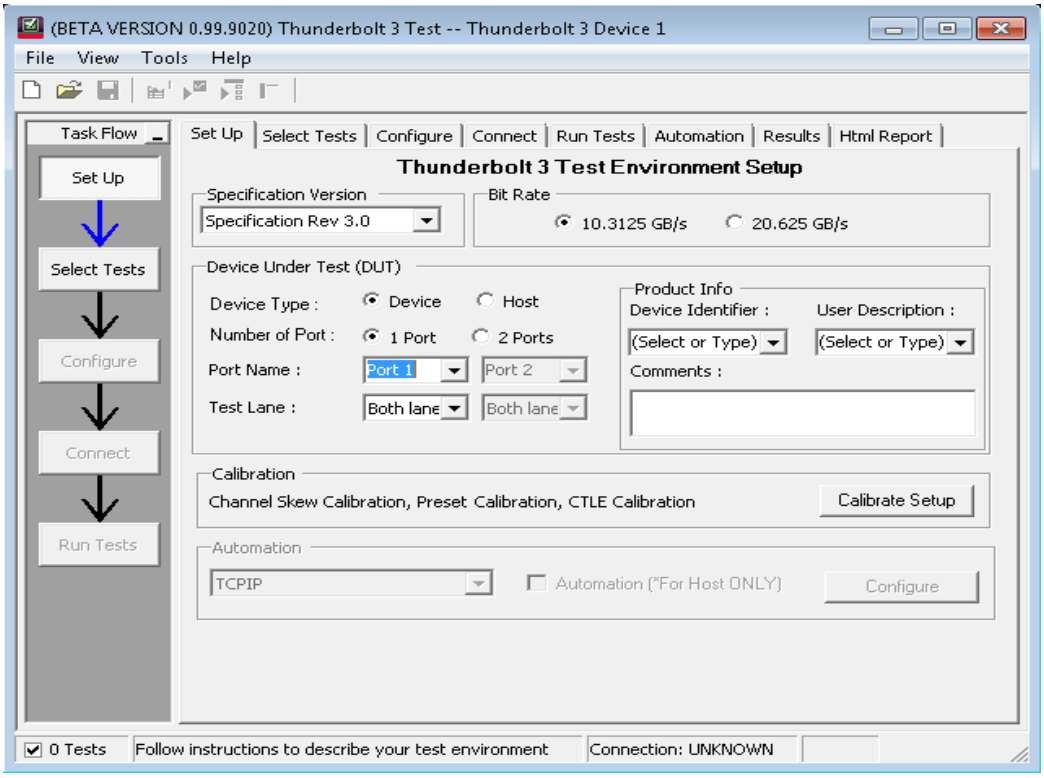


Figure 2 The Thunderbolt Electrical Compliance Test Application's default window

Figure 1 shows the procedure to launch the Thunderbolt 3 Electrical Compliance Test Application and Figure 2 shows the Thunderbolt 3 Electrical Compliance Test Application default window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you identify and set up the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters. This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automation	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE The configuration options shown under the **Set Up** tab of the Thunderbolt Electrical Compliance Test Application main window dictate the availability of various tests.

Online Help Topics

For information on using the Thunderbolt 3 Electrical Compliance Test Application, see its Online Help (which you can access by choosing **Help>Contents**... from the application's main menu).

The Thunderbolt 3 Electrical Compliance Test Application's Online Help describes:

- Starting the Thunderbolt 3 Electrical Compliance Test Application.
- Creating or opening a test project.
- Setting up the Thunderbolt test environment.
- Selecting tests.
- Configuring selected tests.
- Defining compliance limits.
- Connecting the oscilloscope to the device under test (DUT).
- Running tests.
- Automating the application.
- Viewing test results.
- Viewing/exporting/printing the HTML test report.
- Saving test projects.
- Installing/removing add-ins.
- Controlling the application via a remote PC.
- Using a second monitor.

3 Host / Device Thunderbolt 3 Transmitter Testing

The Keysight N6470A Thunderbolt 3 Electrical Compliance Test Application enables compliance testing of the Host and Device Transmitter systems operating at bit rates of either 10.3125 GB/s or 20.625 GB/s; based on *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification version 1.5*.

System Components in Thunderbolt 3 Technology

The following section help you understand an overview of the system components associated with Transmitter testing in the Thunderbolt Technology.

Overview

The flexible networking architecture of the Thunderbolt Technology permits a range of system Devices to be constructed. The Thunderbolt Technology link is characterized by its Thunderbolt Technology connector ports operating either as “Upstream” (i.e. pointing towards a Host) or “Downstream” (pointing towards an Endpoint). When connected and configured, a network of Thunderbolt Technology links shall form a tree topology with the upstream ports leading to a Thunderbolt Host at the root of the tree. For example, a Thunderbolt Device may exchange information with the Thunderbolt Host on its upstream Thunderbolt Technology connector, and may act as a conduit for information between the Host and Devices connected, directly or indirectly, to its downstream port(s). See Figure 3.

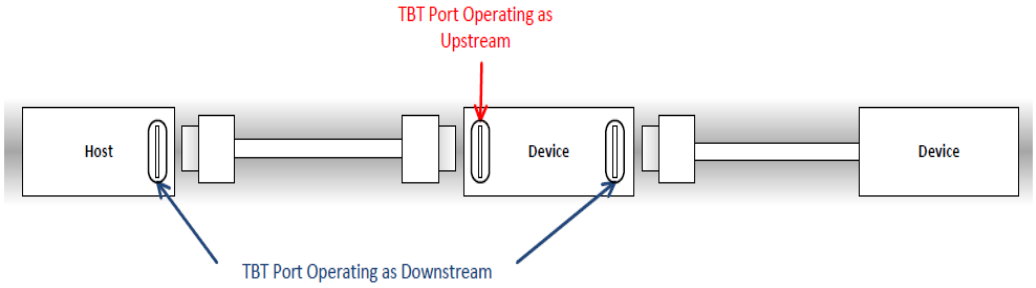


Figure 3 Thunderbolt Technology Link Connection Block Diagram

Two Thunderbolt Host systems may be connected directly which results in an inter-domain connection. An inter-domain connection is also referred to as a peer-to-peer connection. An inter-domain connection can also occur when two downstream ports, which are leaves of two different Host trees are connected. In the inter-domain connection case, the Host systems communicate with each other using memory to memory transactions and the system software configures the connections for the Thunderbolt network, for example, DisplayPort connections. Similarly, PCIe transactions to Devices are carried out with the Host in their respective tree. See Figure 4.

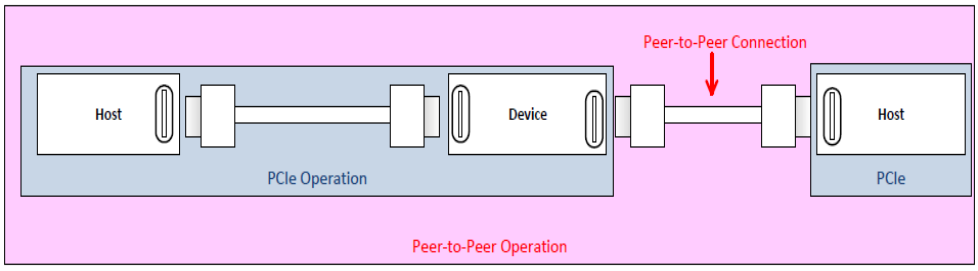


Figure 4 Thunderbolt Technology Peer-to-Peer Connection Block Diagram

The components which support the Thunderbolt Technology link are: a Thunderbolt Host, a Thunderbolt Display, a Thunderbolt Adapter and a Thunderbolt Application Device. A Thunderbolt Display, a Thunderbolt Adapter or a Thunderbolt Application Device are generically referred to as Thunderbolt Devices.

Thunderbolt Host

This component is a usually a computer. A Thunderbolt Host has one or more “Downstream” Thunderbolt Technology connector ports, but no “Upstream” Thunderbolt Technology connector ports. However, Thunderbolt Hosts can be connected peer-to-peer. A Thunderbolt Host provides the role of Thunderbolt network discovery and configuration. There shall be at least one Thunderbolt Host in a Thunderbolt network. A Thunderbolt network with more than one Thunderbolt Host can provide peer-to-peer communications between the Thunderbolt Hosts present on the network. A Thunderbolt Host Type-C includes the following:

- A Thunderbolt Controller, which contains one or more DisplayPort input interfaces, a PCI Express interface, and one or more Thunderbolt Technology interfaces.
- A multiplexer, which selects either Thunderbolt, DP v1.2, or USB r3.1 data. The multiplexer is integrated into the 3rd Generation TBT Controller.
- A Link Controller with a UART interface for managing operation and power states of the Thunderbolt link when in the Thunderbolt Alternate Mode. The Link Controller is integrated into the 3rd Generation TBT Controller.
- A USB PD Port Controller implemented as a DRP with the ability to support the Thunderbolt and DisplayPort Alternate Modes.
- At least one USB Type-C connector.

Table 2 lists the Thunderbolt Host rules in conjunction with the USB Type-C connector.

Table 2 Thunderbolt Host Rules with USB Type-C connector

Technology	Thunderbolt Host Rules
USB	▪ Hosts shall support USB r3.1 gen1 and gen2. Hosts shall support USB r2.0. ▪ Hosts shall support USB PD and Biphase Mark Coding. ▪ Hosts shall provision power as defined in Section 7.3 of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification version 1.5*.
Thunderbolt	▪ Hosts shall support 3rd Generation TBT with the USB Type-C connector. ▪ Hosts shall support the pin mapping as defined in Section 7.5.1 of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification version 1.5*.
PCIe	▪ Hosts shall connect PCIe to the Thunderbolt Controller. ▪ One port Hosts are recommended to connect 4-lanes of PCIe Gen3 to the Thunderbolt Controller. ▪ One port Hosts shall connect at least 2-lanes of PCIe Gen3 to the Thunderbolt Controller. ▪ Two port Hosts shall connect 4-lanes of PCIe Gen3 to the Thunderbolt Controller. ▪ Hosts shall support PCIe hot plug.
DisplayPort	▪ Hosts shall redrive DisplayPort from the Thunderbolt Controller to the USB Type-C connector. ▪ One port Thunderbolt Hosts are recommended to connect two DP v1.2 streams (4-lanes each) to the Thunderbolt Controller. ▪ One port Thunderbolt Hosts shall connect at least one DP v1.2 stream (4-lanes) to the Thunderbolt Controller. ▪ Two port Thunderbolt Hosts shall connect at least two DP v1.2 streams (4-lanes each) to the Thunderbolt Controller. ▪ Hosts shall support the pin mapping as defined in Section 7.5.2 of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification version 1.5*.

Thunderbolt Device

A Thunderbolt Device has at least one port that is capable of operating as an “Upstream” port and contains a Thunderbolt Controller and optionally a PCIe to I/O Bridge to another interface such as FireWire, Ethernet, or eSATA. The Thunderbolt Device may present the other interface connector or may include internal functionality that is appropriate to a device. Thunderbolt Controllers contain some PCIe to I/O bridging capabilities and additional I/O Bridge chips may not be needed. You may refer to the appropriate Thunderbolt Controller datasheet for more information.

When the Thunderbolt Device is connected to the Thunderbolt Host, the bridge chip functions as if it were connected directly to the Host's PCIe bus. A Thunderbolt Device with a downstream port, shall provide DP v1.2 support or USB r3.1 support in the case where a USB Type-C cable and a USB or DP Device are connected. Examples of Thunderbolt Devices include a PCIe expansion chassis or a RAID array controller, a Thunderbolt to FireWire adapter, a Thunderbolt to Ethernet adapter, a Thunderbolt Display and so on.

A Thunderbolt Device may have one or more ports, which can operate as "Downstream" port(s). A Thunderbolt Device may or may not have a Thunderbolt cable permanently attached. A Thunderbolt Device with a Thunderbolt cable permanently attached is called a Tethered Device.

Thunderbolt Display—A Thunderbolt Display is a specific type of Thunderbolt Device. A Thunderbolt Display has at least one port, which is capable of operating as an Upstream Thunderbolt Technology connector port and an integrated display which shall display DisplayPort format information tunneled through the Thunderbolt Technology link. A Thunderbolt Display may also have a second port operating as a "Downstream" port. Downstream ports operate as the Thunderbolt Technology connector ports and optionally support USB r3.1 when a USB device is connected or DP on Type-C when a DisplayPort adapter is connected. A Thunderbolt Display may also contain PCIe subsystems connected to the Thunderbolt Controller's PCIe interface, for example a Gigabit Ethernet controller.

Thunderbolt Links and Lanes

A link is defined as one or more dual-simplex communication paths between two Thunderbolt Controllers. A link may be composed of multiple lanes or channels. A link is symmetric in that each direction of the link shall support the same number of lanes and each lane shall operate at the same signaling rate.

A lane is composed of two differential signal pairs, one transmitting and one receiving. Each differential pair operates at a signaling rate which defines the speed of communication for that lane. Multiple lanes may be aggregated (bonded) to scale bandwidth. The Thunderbolt Technology connector can be connected to 1 or 2 Thunderbolt Lanes, depending on the implementation or Thunderbolt rules.

3rd Generation Thunderbolt Electrical Compliance Methodology

System Compliance Test Point Definitions

The 3rd Generation Thunderbolt defines the following reference points for compliance testing of Host/Device Thunderbolt Transmitter Systems:

1 TP1—Reference measurement point located at the plug side of the Host/Device Transmitter output. Used as a reference point for defining the Host/Device Transmitter and the Active Cable/Adapter Receiver specifications.

2 TP2—Reference measurement point located at the plug side of the Host/Device Receiver input. Used as a reference point for defining the Active Cable/Adapter Transmitter and the Host/Device Receiver specifications.

3 TP3EQ—Reference measurement point located at the far-end side of a passive cable or at the output of a tethered device. Used as a reference point for passive installations and tethered devices. All the measurements at this point are done after applying reference equalization.

For Host / Device Transmitter testing, all measurements shall be referenced to the TP1/TP3EQ compliance points defined above and as shown in Figure 5. Calibration shall be applied in cases where direct measurement at TP1 is not feasible.

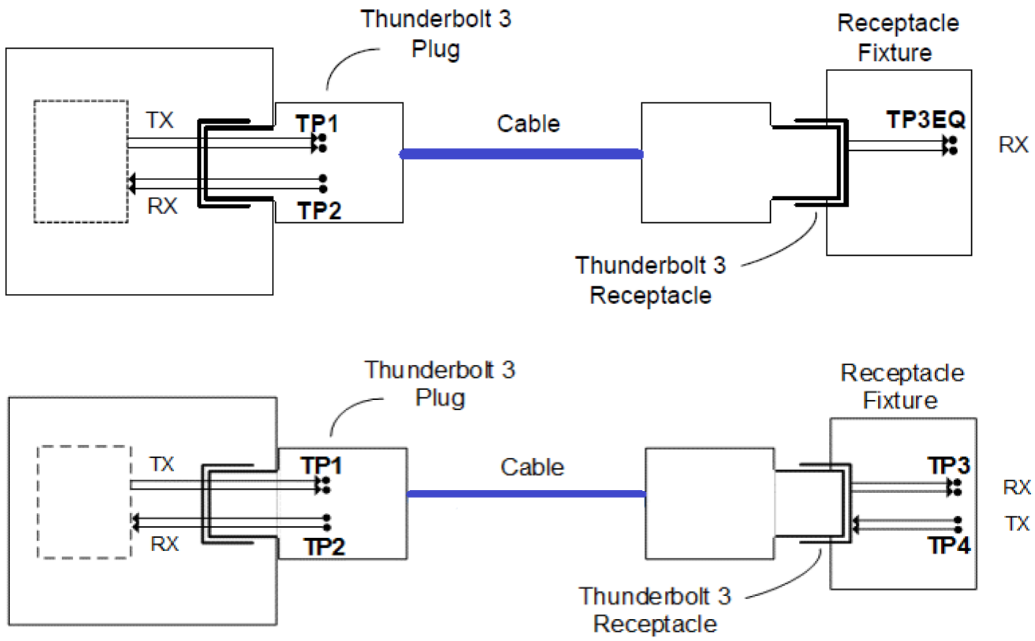


Figure 5 Thunderbolt Compliance Points Definition

AC Coupling Capacitors

The high speed electrical interfaces shall be AC-coupled. The Host/Device transmit paths shall include AC-coupling capacitance between 165nF and 265nF. In addition, the plugs of the Active Cable and the Tethered Device should include AC-coupling capacitance between 165nF and 265nF placed at their output transmit path. Capacitors shall not be placed on the high-speed receiver paths of the different 3rd Generation Thunderbolt components.

Jitter and Eye Measurement Methodology

The Thunderbolt jitter and eye diagram specifications are all referenced to a golden clock-and-data recovery (CDR) function, meaning that all measurements shall be performed after applying appropriate tracking on the signal's phase. The reference CDR is modeled by a 2nd order PLL response (type II), which derives the following jitter rejection mask, described in Laplace domain, as described in Figure 6:

$$H_{jitter}(s) = \frac{s^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + {\omega_n}^2}$$

Where:

$s = j \cdot 2 \cdot \pi \cdot f$, ζ *is the damping factor,* ω_n *is the natural frequency of the system*

Figure 6 Jitter Rejection Mask described in Laplace domain

Table 3 defines the 3rd Generation Thunderbolt Reference CDR Parameters:

Table 3 3rd Generation Thunderbolt Reference CDR Parameters

Speed	Damping Factor	Natural Frequency - [rad/sec]
10.3125 Gb/s	0.94	2.2e7 rad/sec
20.625 Gb/s	0.71	3.1e7 rad/sec

Figure 7 shows the Thunderbolt 3.0 CDR Jitter Rejection Mask Plot for 10.3125 GB/s and 20.625 GB/s:

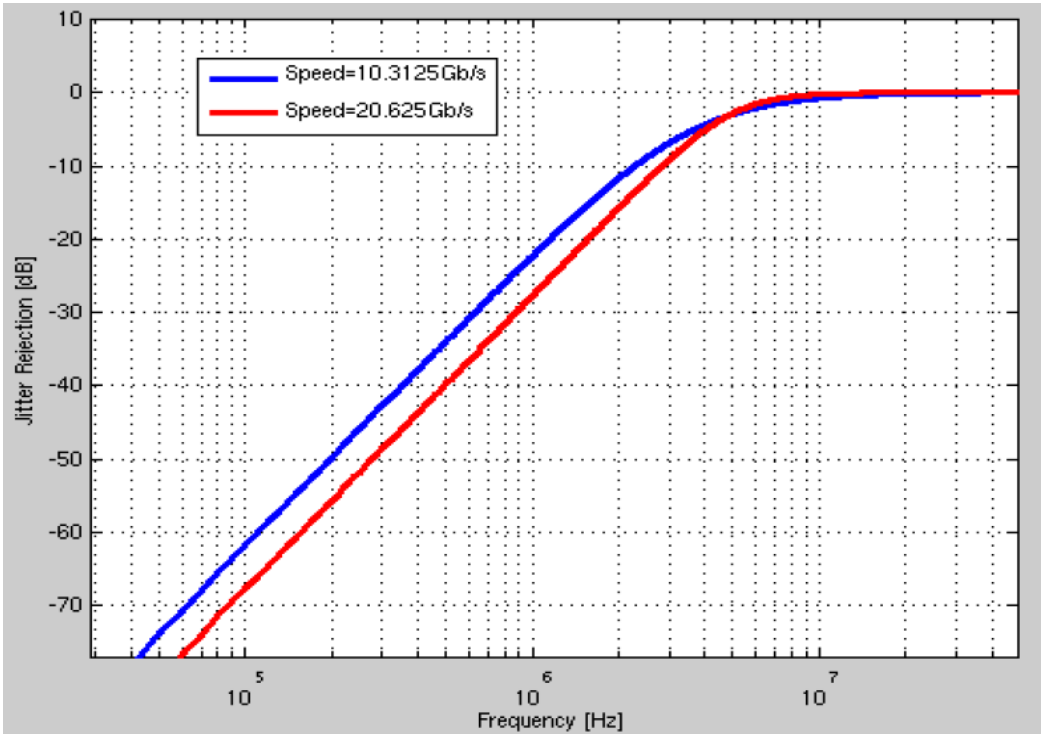


Figure 7 3rd Generation Thunderbolt Jitter Rejection Mask

Reference Equalization Function

All the measurements done at the output of the cable assembly, denoted as TP3EQ, should be referenced to a golden receiver equalization function, that is, all measurements shall be performed after applying appropriate equalization on the measured signals. The reference receiver applied at TP3EQ comprises of parametric Continuous-Time-Linear-Equalizer (CTLE) and Decision-Feedback-Equalizer (DFE), as described in Figure 7. For each measurement referenced to TP3EQ, make sure to set the best equalization parameters such that the calculated eye-diagram is optimized.

Reference CTLE

The equation, shown in Figure 8, describes the frequency response for the 3rd Generation Thunderbolt continuous time linear equalizer that must be used for compliance testing:

$$H(s) = 1.41 \cdot w_{p2} \cdot \frac{s + \frac{A_{DC}}{1.41} \cdot w_{p1}}{(s + w_{p1}) \cdot (s + w_{p2})}$$

Where:

A_{DC} *is the DC gain*

$$w_{p1} = \begin{cases} 2 \cdot \pi \cdot 1.5e9 \ \frac{rad}{Sec} & Speed = 10.3125\ Gb/s \\ 2 \cdot \pi \cdot 5e9 \ \frac{rad}{Sec} & Speed = 20.625\ Gb/s \end{cases}$$

$$w_{p2} = \begin{cases} 2 \cdot \pi \cdot 5e9 \ \frac{rad}{Sec} & Speed = 10.3125\ Gb/s \\ 2 \cdot \pi \cdot 10e9 \ \frac{rad}{Sec} & Speed = 20.625\ Gb/s \end{cases}$$

$s = j \cdot 2 \cdot \pi \cdot f$ *is the frequency in Laplace domain*

Figure 8 Frequency Response Equation for 3rd Generation TBT CTLE

Apply ten different CTLE configurations such that the value of A_{DC} is one of $\{10^{-x/20} : x = 0 \div 9\ [dB]\}$.

and show the Frequency Response of the 3rd Generation Thunderbolt Reference CTLE for 10.3125 GB/s Systems and for 20.625 GB/s systems, respectively.

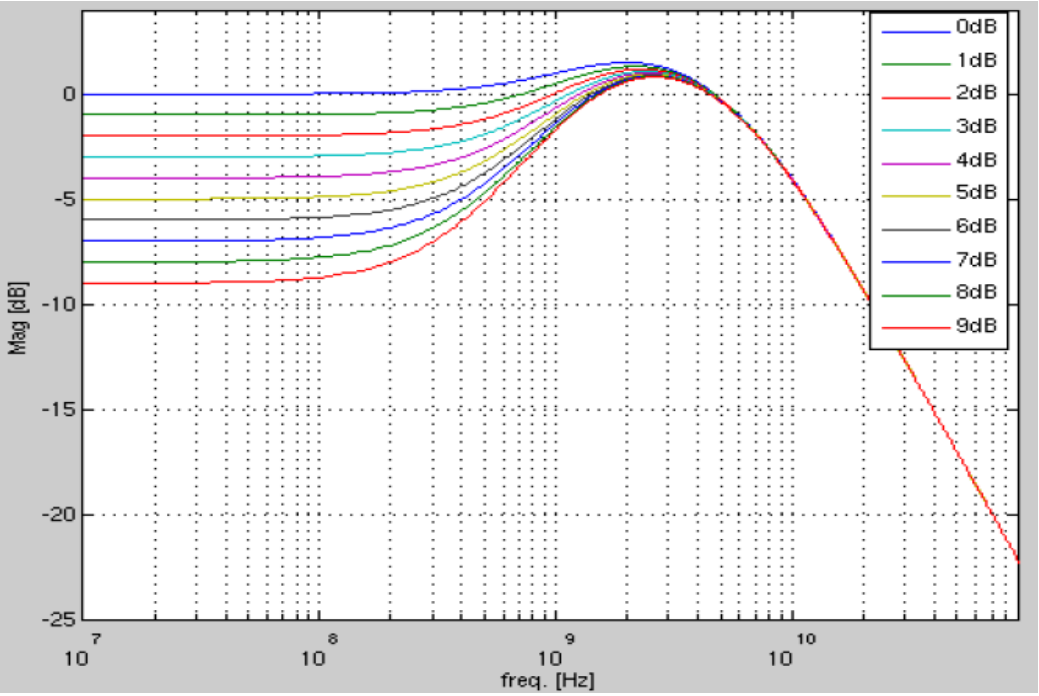


Figure 9 Thunderbolt 3 Reference CTLE for 10.3125 Gbps Systems

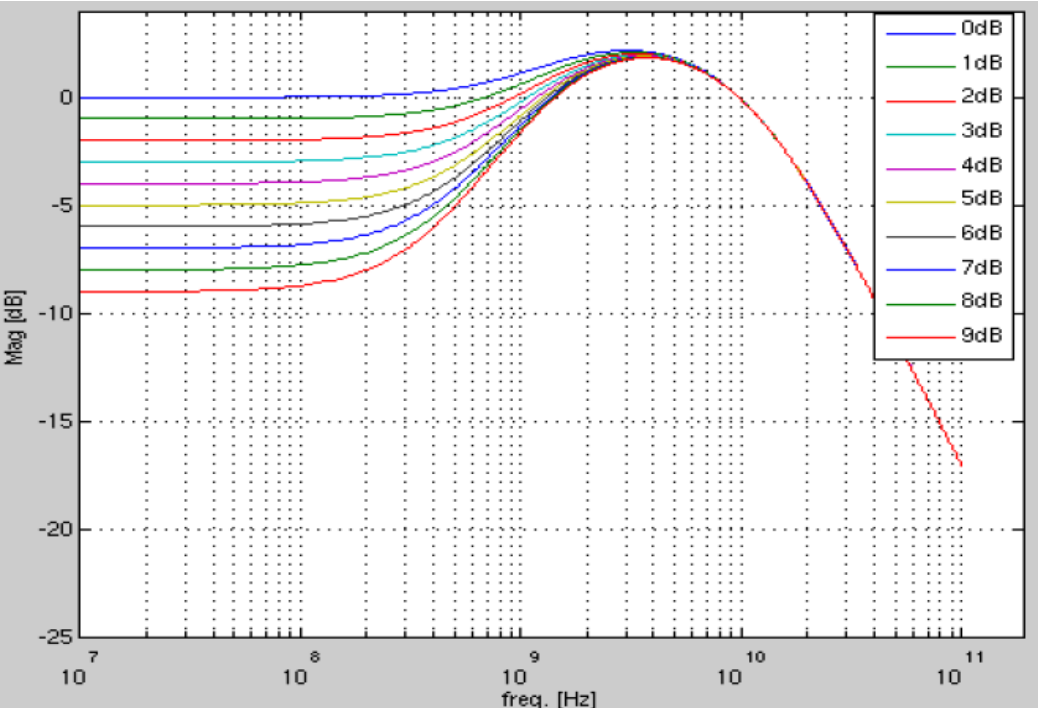


Figure 10 Thunderbolt 3 Reference CTLE for 20.625 Gbps Systems

Reference DFE

A 1-tap reference feedback filter is defined as part of the reference receiver equalizer used in the compliance testing. The DFE formula is described in the equation, shown in Figure 11.

$$y_n = x_n - c_1 \cdot sign(y_{n-1})$$

Where:

y_n *is the DFE output at time instant n*

x_n *is the DFE input (incoming signal after applying the CTLE)*

c_1 *is the DFE coefficient, which may get values between 0 to 50mV.*

Figure 11 3rd Generation Thunderbolt Decision-Feedback-Equalizer (DFE) Formula

Figure 12 shows the flowchart representation of the Reference Receiver Equalization.

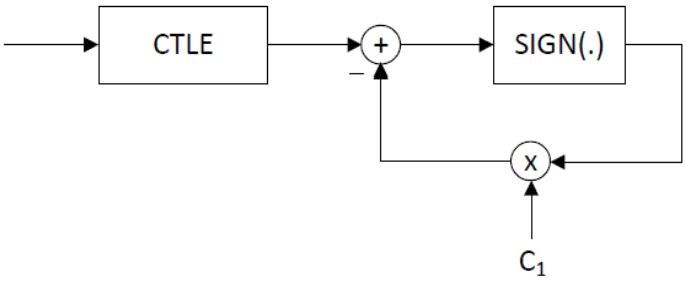


Figure 12 3rd Generation Thunderbolt Reference Receiver Equalization

Requirements for Host / Device Transmitter Compliance

The 3rd Generation TBT Host/Device transmitter compliance test is defined at the output of a “golden” plug fixture (TBT3-P) at point TP1 and at the output of a “golden” receptacle fixture (TBT3-R) at point TP3EQ. For more information about the reference test boards TBT3-P and TBT3-R, refer to Section 5.6.3 and Section 5.7.5 of *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification version 1.5*.

The Host/Device Transmitter shall transmit a PRBS31 pattern during the compliance testing, except when testing specific parameters that require dedicated patterns that are explicitly defined in the specific context. The test shall be performed while the Spread-Spectrum-Clocking (SSC) is enabled, and while the neighbor interfaces are active.

Host / Device Transmitter Specifications for both 10.3125 GB/s and 20.625 GB/s Systems

Table 4 defines parameters for the 3rd Generation TBT Host/Device Transmitters, which apply for both 10.3125 GB/s and 20.625 GB/s systems.

Table 4 Common Host / Device Transmitter Specifications at TP1

Symbol	Description	Min	Max	Units	Comments
TX_EQ	Transmitter Equalization	See “Transmit Equalization" on page 37	–	–	–
SSC_DOWN_SPREAD_DEVIATION	SSC down-spreading deviation	-0.03	0.53	%	0% to 0.5% with 300ppm tolerance
SSC_DOWN_SPREAD_RATE	SSC down-spreading modulation rate	35	37	KHz	–
SSC_PHASE_DEVIATION	Phase jitter associated with the SSC modulation	2.5	16.5	ns pp	See Note 1
SSC_PHASE_SLEW_RATE	SSC Phase Jitter Slew Rate	–	3.3	ms/s	See Note 2
RISE_FALL_TIME	TX Rise/Fall time measured between 20-80% levels	10	–	ps	Test Pattern shall be alternating square pattern of sixteen 0’s and sixteen 1’s

Note:

1. The SSC phase deviation shall be extracted from the transmitted signal. During this test, the transmitter shall be configured to send PRBS31 pattern. The SSC phase deviation is the signal phase jitter after applying a 2nd order low-pass filter with 3dB point at 5MHz.
2. The SSC phase slew rate shall be extracted from the transmitted signal. During this test, the transmitter shall be configured to send PRBS31 pattern. The SSC phase slew-rate shall be extracted from the phase jitter after applying a 2nd order low-pass filter with 3dB point at 5MHz.

Transmit Equalization

The 3rd Generation Thunderbolt Host/Device implements coefficient based equalization at its transmitter. The transmit equalization should support 16 specified preset covering different de-emphasis and pre-shoot configurations. The equalizer's structure is based on UI-spaced 3 tap finite-impulse-response (FIR) filter as shown in Figure 14. The transmitted level corresponding to the nth symbol is calculated using the equation shown in Figure 13:

$$tx\_out_n = \sum_{k=-1}^{1} data\_in_{n-k} \cdot C_k$$

Figure 13 Transmit Equalization equation for transmitted levels corresponding to the nth symbol

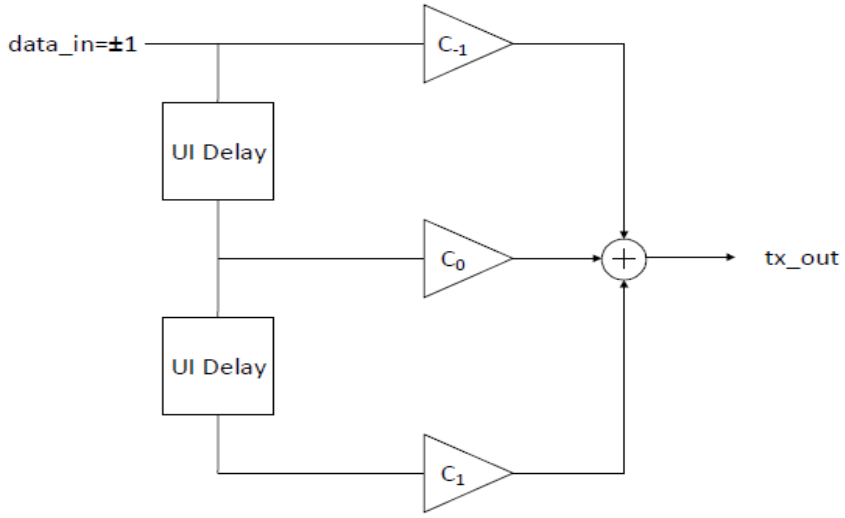


Figure 14 Transmitter Equalizer Structure

Table 5 indicates the normative Pre-shoot and De-emphasis requirements of the transmitter equalization presets and the corresponding informative coefficients values.

Preset configurations 0 to 14 represent operation mode with full-swing transmitter output while configuration 15 represents the low-swing mode. When you select configuration 15, the transmitter's output swing should be attenuated by 3.5±1dB compared to its full-swing operation. The required tolerance of the Pre-shoot and De-emphasis is ±1dB.

Table 5 Transmit Equalization Presets

Preset Number	Pre-Shoot [dB]	De-Emphasis	Informative Filter Coefficients		
			C_{-1}	C_0	C_1
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.7	0	0.76	-0.24
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	4.3	-9.3	-0.09	0.64	-0.27
15	1.7	-1.7	-0.05	0.55	-0.05

Note:

1. The coefficients are normalized such that $|C_{-1}|+C_0+|C_1|$ correspond to full output swing. Preset configuration 15 represent operation mode with lower transmitter swing.

2. Pre-Shoot and De-Emphasis are calculated using the equations shown in Figure 15:

$$Preshoot = 20 \cdot log_{10}\left(\frac{-C_{-1}+C_0+C_1}{C_{-1}+C_0+C_1}\right)$$

$$De-emphasis = 20 \cdot log_{10}\left(\frac{C_{-1}+C_0+C_1}{C_{-1}+C_0-C_1}\right)$$

Figure 15 Equations to calculate Pre-Shoot and De-Emphasis

Figure 16 depicts the corresponding frequency responses of the different transmit equalization presets for 10.3125 GB/s and 20.625 GB/s speeds of operation:

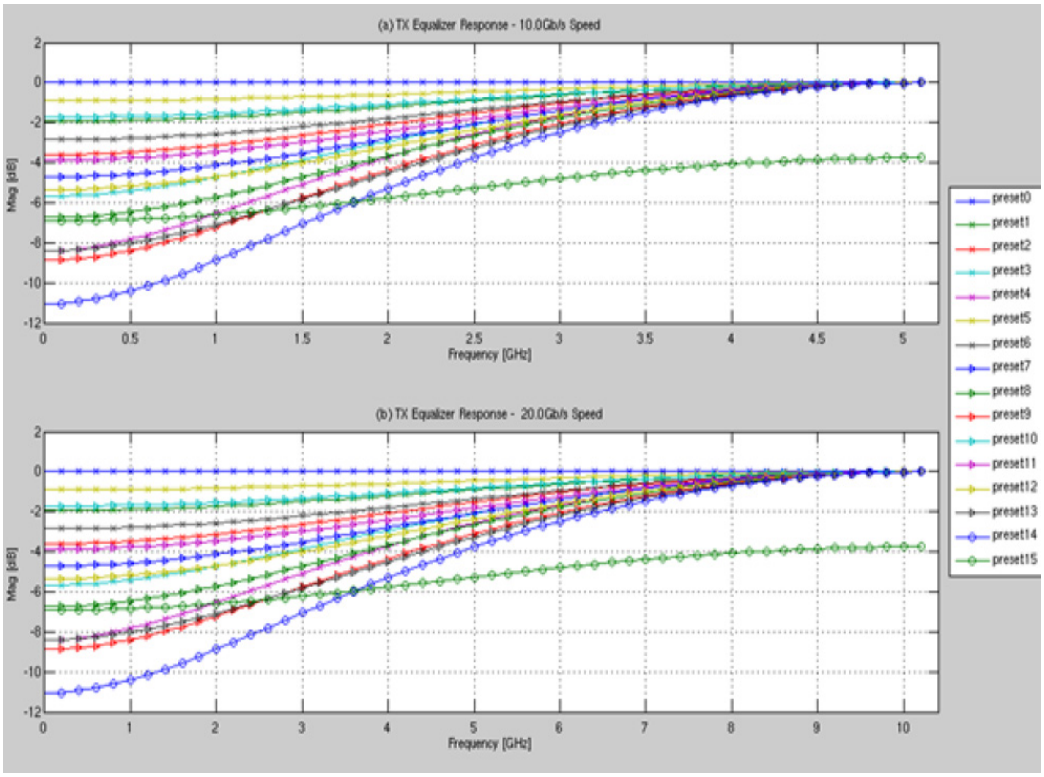


Figure 16 Transmitter Equalizer Frequency Response

Dedicated Host / Device Transmitter Compliance Specifications for 10.3125 GB/s Connections

Table 6 and Table 7 define the required specifications for 10.3125 GB/s Host/Device transmitter. The following tables shall be met in addition to Table 4, which covers 10.3125 GB/s transmitter parameters as well. Table 7 should be measured after applying the reference receiver equalization function defined in “Reference Equalization Function" on page 33.

Table 6 10.3125 GB/s Host / Device Transmitter Specifications at TP1

Symbol	Description	Min	Max	Units	Comments
UI	Unit Interval	96.9406	97.4864	ps	Frequency high limit = +300 ppm Frequency low limit = -5300 ppm See Note 4
UI_MEAN	Average Unit Interval	97.1835	97.2419	ps	See Note 5
AC_CM	TX AC Common Mode Voltage	–	100	mV pp	See Note 2
TJ	Total Jitter	–	0.38	UI pp	See Notes 2, 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	–	0.31	UI pp	See Notes 2, 3
UDJ	Uncorrelated Deterministic Jitter	–	0.17	UI pp	See Notes 2, 3
X1	TX eye horizontal opening	–	0.19	UI	Measured for 1e-6 Mask Hit Ratio. See Notes 2, 7 and Figure 17
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	180	–	mV	Measured for 1e-6 Mask Hit Ratio. See Notes 1, 2 and Figure 17
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	–	700	mV	Measured for 1e-6 Mask Hit Ratio. See Notes 1, 2 and Figure 17

Note:

1. TX voltage is differential.
2. Measured while applying the reference CDR described in “Jitter and Eye Measurement Methodology” on page 32.
3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS.
4. UI shall be calculated dynamically using a uniform moving average filter with window size of 3000 symbols.
5. The average UI shall be measured over windows at the size of one SSC cycle.
6. The test shall be performed while the SSC is enabled while the neighbor interfaces are active.
7. X1 specification is informative and given only as a direction for ensuring that the normative TJ specification is met.

Table 7 10.3125 GB/s Host / Device Transmitter Specifications at TP3EQ

Symbol	Description	Min	Max	Units	Comments
TJ	Total Jitter	–	0.66	UI pp	See Notes 2, 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	–	0.33	UI pp	See Notes 2, 3
UDJ	Uncorrelated Deterministic Jitter	–	0.17	UI pp	See Notes 2, 3
X1	TX eye horizontal opening	–	0.33	UI	Measured for 1e-6 Mask Hit Ratio. See Notes 2, 6 and Figure 17
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	35	–	mV	Measured for 1e-6 Mask Hit Ratio. See Notes 1, 2 and Figure 17
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	–	1000	mV	Measured for 1e-6 Mask Hit Ratio. See Notes 1, 2 and Figure 17

Note:

1. TX voltage is differential.
2. Measured while applying the reference CDR described in “Jitter and Eye Measurement Methodology” on page 32 and the reference equalizer defined in “Reference Equalization Function” on page 33.
3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS.
4. All transmitters should be active during the test (both in the near-end and the far-end sides).
5. All measurements should be done after applying Reference Receiver Equalization defined in “Reference Equalization Function” on page 33.
6. X1 specification is informative and given only as a direction for ensuring that the normative TJ specification is met.

Figure 17 shows the Host / Device Transmitter Eye Mask Notations, defined in the tables above.

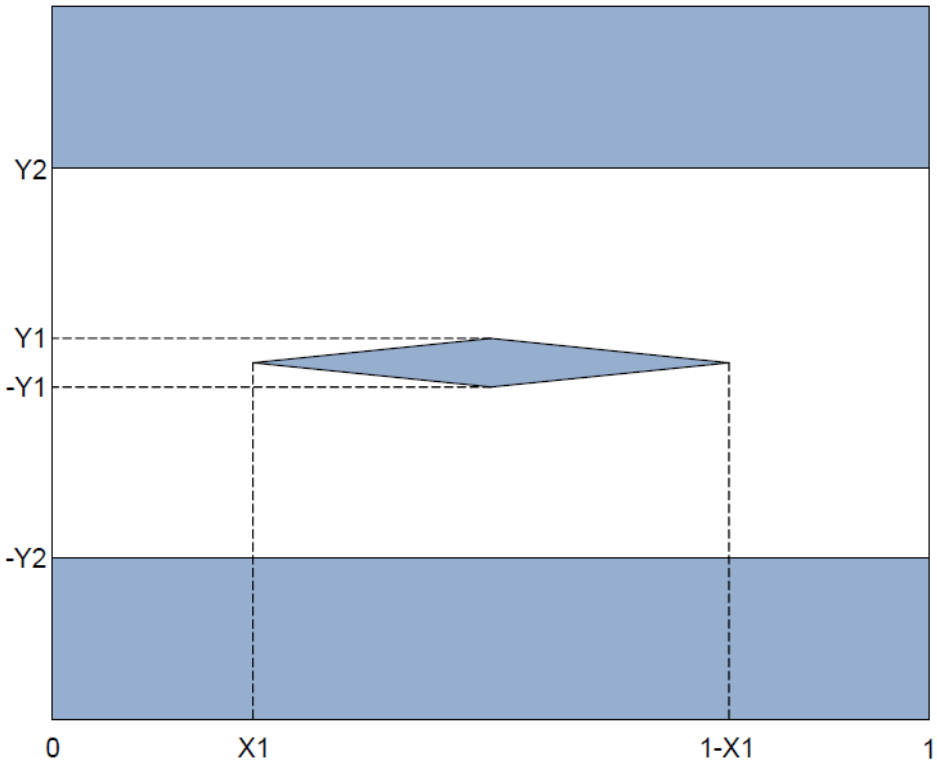


Figure 17 Host / Device TX Mask Notations

Dedicated Host / Device Transmitter Compliance Specifications for 20.625 GB/s Connections

Table 8 and Table 9 define the required specifications for 10.3125 GB/s Host/Device transmitter. The following tables shall be met in addition to Table 4, which covers 10.3125 GB/s transmitter parameters as well. Table 9 should be measured after applying the reference receiver equalization function defined in "Reference Equalization Function" on page 33.

Table 8 20.625 GB/s Host / Device Transmitter Specifications at TP1

Symbol	Description	Min	Max	Units	Comments
UI	Unit Interval	48.4703	48.7432	ps	Frequency high limit = +300 ppm Frequency low limit = -5300 ppm See Note 4
UI_MEAN	Average Unit Interval	48.5917	48.6210	ps	See Note 6
AC_CM_LOW_SWING	TX AC Common Mode Voltage for systems with peak inner eye < 100mV	–	80	mV pp	Maximum allowed ACCM voltage for systems with low output swing
AC_CM_HIGH_SWING	TX AC Common Mode Voltage for systems with peak inner eye > 100mV	–	100	mV pp	Maximum allowed ACCM voltage for systems with high output swing
TJ	Total Jitter	–	0.50	UI pp	See Notes 2, 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	–	0.31	UI pp	See Notes 2, 3
UDJ	Uncorrelated Deterministic Jitter	–	0.17	UI pp	See Notes 2, 3
X1	TX eye horizontal opening	–	0.275	UI	Measured for 1e-6 Mask Hit Ratio. See Notes 2, 7 and Figure 17
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	120	–	mV	Measured for 1e-6 Mask Hit Ratio. See Notes 1, 2 and Figure 17
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	–	700	mV	Measured for 1e-6 Mask Hit Ratio. See Notes 1, 2 and Figure 17

Note:

1. TX voltage is differential.
2. Measured while applying the reference CDR described in "Jitter and Eye Measurement Methodology" on page 32.
3. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS.
4. UI shall be calculated dynamically using a uniform moving average filter with window size of 6000 symbols.
5. The average UI shall be measured over windows at the size of one SSC cycle.
6. SS shall be enabled during all tests.
7. X1 specification is informative and given only as a direction for ensuring that the normative TJ specification is met.

Table 9 "Preliminary" 20.625 GB/s Host / Device Transmitter Specifications at TP3EQ

Symbol	Description	Min	Max	Units	Comments
TJ	Total Jitter	–	0.66	UI pp	See Notes 2, 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	–	0.33	UI pp	See Notes 2, 3
UDJ	Uncorrelated Deterministic Jitter	–	0.17	UI pp	See Notes 2, 3
X1	TX eye horizontal opening	–	0.33	UI	Measured for 1e-6 Mask Hit Ratio. See Notes 2, 5 and Figure 17
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	35	–	mV	Measured for 1e-6 Mask Hit Ratio. See Notes 1, 2 and Figure 17
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	–	1000	mV	Measured for 1e-6 Mask Hit Ratio. See Notes 1, 2 and Figure 17

Note:

1. TX voltage is differential.
2. Measured while applying the reference CDR described in "Jitter and Eye Measurement Methodology" on page 32 and the reference equalizer defined in "Reference Equalization Function" on page 33.
3. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS.
4. All transmitters should be active during the test (both in the near-end and the far-end sides).
5. X1 specification is informative and given only as a direction for ensuring that the normative TJ specification is met.

Transmitter Test Setup

Figure 18 shows the typical connections to the DUT and the control PC (if any) used for Host / Device Transmitter testing for both 10.3125 GB/s and 20.625 GB/s Systems. During the test runs, if required, the Thunderbolt Electrical Compliance Test Application prompts for changes in connection setup.

NOTE **Before you begin any tests or data acquisition, ensure that the Oscilloscope is warmed, calibrated and the cables de-skewed. See "Calibrating the Infiniium Oscilloscope" on page 159.**

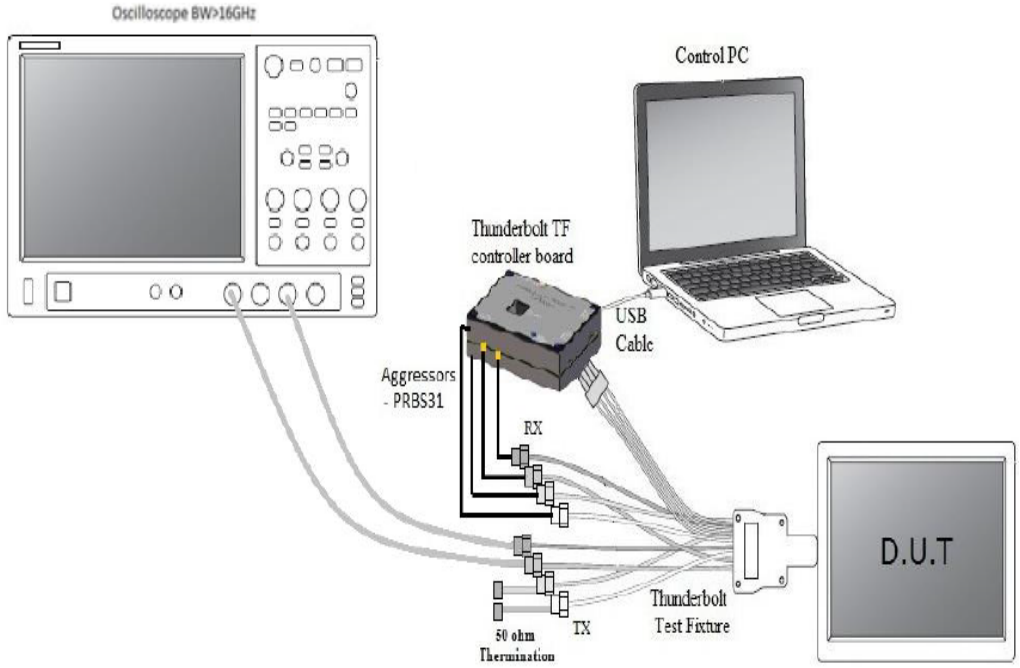


Figure 18 Thunderbolt 3 Host / Device Transmitter Common Test Setup

Connecting to the DUT

1 Connect the Lane under test TX_P, TX_N to the Oscilloscope.
2 Connect termination to the TX Lane, which is not under test.
3 Connect the RX Lanes to Thunderbolt Micro-Controller SMA Lanes, 800mV amplitude to inject crosstalk.

4 Transmitter Tests for 10.3125 GB/s Systems

This section provides the Methods of Implementation (MOIs) to run electrical tests on a Thunderbolt DUT operating at a bit rate of 10.3125 GB/s using an Keysight Infiniium Oscilloscope and other accessories, along with the Thunderbolt 3 Electrical Compliance Test Application.

Setting Up Test Application for 10.3125 GB/s Systems

In order to run the electrical compliance tests on a Thunderbolt DUT operating at a bit rate of 10.3125 GB/s, you must set up the Thunderbolt Electrical Compliance Test Application to be able to view and select the required tests. To set up the Thunderbolt Electrical Compliance Test Application:

1 Start the Thunderbolt Electrical Compliance Test Application. See "Starting the Thunderbolt 3 Electrical Compliance Test Application" on page 23.

2 Under the **Set Up** tab, select the following options, as shown in Figure 19 and Figure 20.

a **Specification Version** – Select **Specification Rev 3.0** from the drop-down. Currently, the Test Application supports only this version.

b **Bit Rate** – Select **10.3125GB/s**.

c **Device Type:** – Select DUT Type as either **Device** (default) or **Host**.

d **Number of Port:** – Select **1 Port (default)** or **2 Ports**. This drop-down field allows you to type a custom name for the ports being used for testing.

e **Test Lane:** – From the drop-down options, select either **Both Lanes** (default), **Lane 0 only** or **Lane 1 only**; depending on the number of lanes being used for testing.

f **Product Info** – Helps you in proper identification of the DUT on HTML reports. This option is particularly useful when running compliance tests on multiple DUTs.

- **Device Identifier :** – Type an appropriate name/identifier for the DUT, which is being tested. The entries are saved such that you may select the values again later, if required.
- **User Description :** – Type an appropriate description for the DUT, which is being tested. The entries are saved such that you may select the values again later, if required.
- **Comments :** – Type appropriate comments, if required.

g **Calibration** – Click the **Calibrate Setup** button to perform **Channel Skew Calibration** and if required, perform either **Preset Calibration** or **CTLE Calibration** or both, before running the respective tests.

- **Channel Skew Calibration** – Required to calibrate Channel Skew on the Oscilloscope Channels where the DUT is connected.
- **Preset Calibration** – Required to run the Transmitter Preset Calibration tests.
- **CTLE Calibration** – Required to run the Transmitter CTLE Calibration and Transmitter Equalization tests.

  See "Calibration Setup for Compliance Tests" on page 55 for more information on these calibration options.

h **Automation** – This feature is enabled only when you select **Device Type :** as **Host**. Use this feature for remote configuration and controlling of a Thunderbolt Host, which is a usually a remote PC or a Thunderbolt Micro-Controller.

  For more information about using this feature, refer to "Automation" under the section "Setting Up the Test Environment" in the *Keysight N6470A Thunderbolt 3 Compliance Test Application Online Help*.

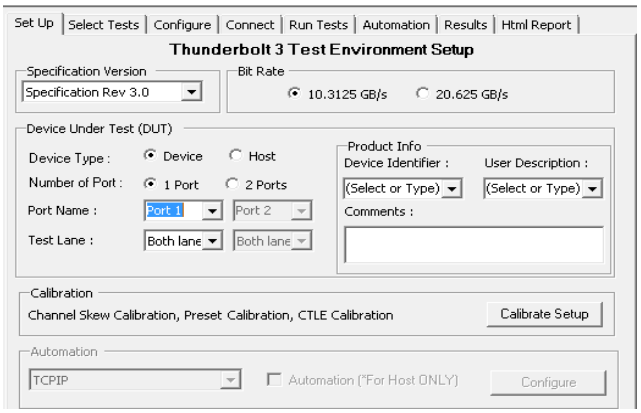


Figure 19 Set Up options for DUT Type “Device” operating at 10.3125 GB/s

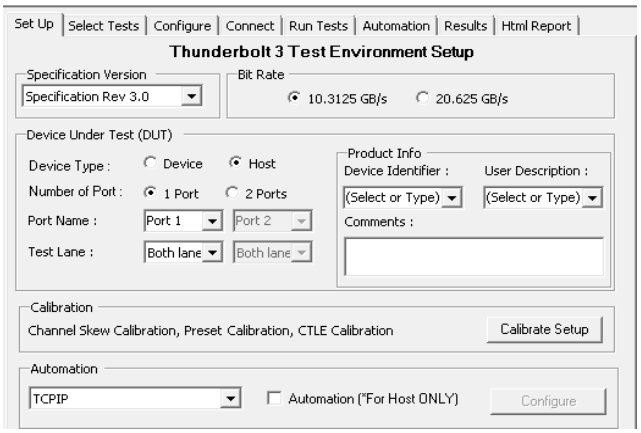


Figure 20 Set Up options for DUT Type “Host” operating at 10.3125 GB/s

3 Based on your choices under the **Set Up** tab, the **Select Tests** tab displays the associated tests. For example, Figure 21 shows the compliance tests for DUT Type “Device” with 1-Port, 2-Lane system and Figure 22 shows the compliance tests for DUT Type “Host” with 1-Port, 2-Lane system. Select the tests that you want to run using the Thunderbolt Electrical Compliance Test Application. Refer to the *Keysight N6470A Thunderbolt Electrical Compliance Test Application Online Help* to know more about how to select tests.

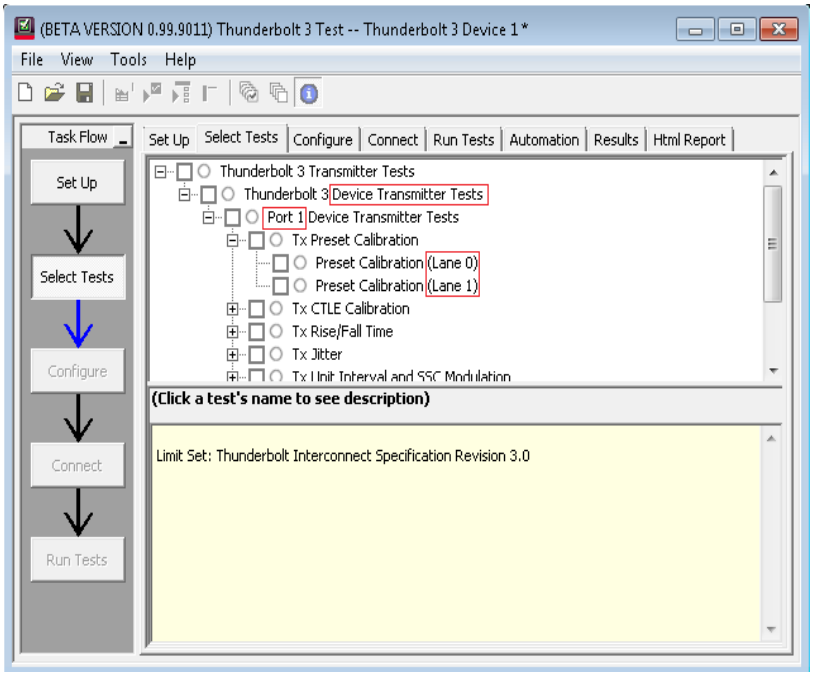


Figure 21 Select Transmitter Tests for DUT Type “Device” on 1-Port, 2-Lanes

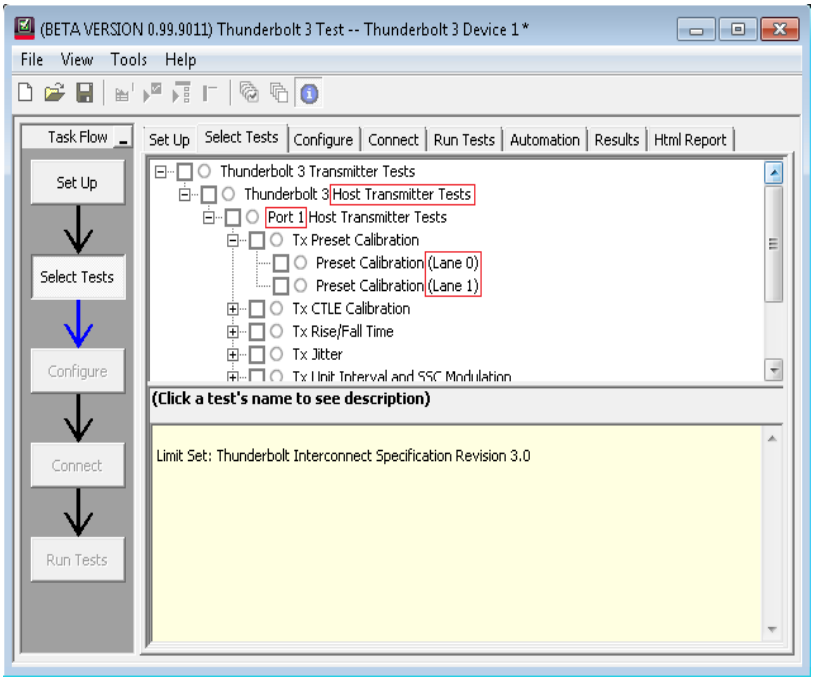


Figure 22 Select Transmitter Tests for DUT Type “Host” on 1-Port, 2-Lanes

4 Under the **Configure** tab, you may modify the values for various configurable options associated with the compliance tests. By default, the Thunderbolt Compliance Test Application sets the values of these options to the optimum value according to the standard specifications.

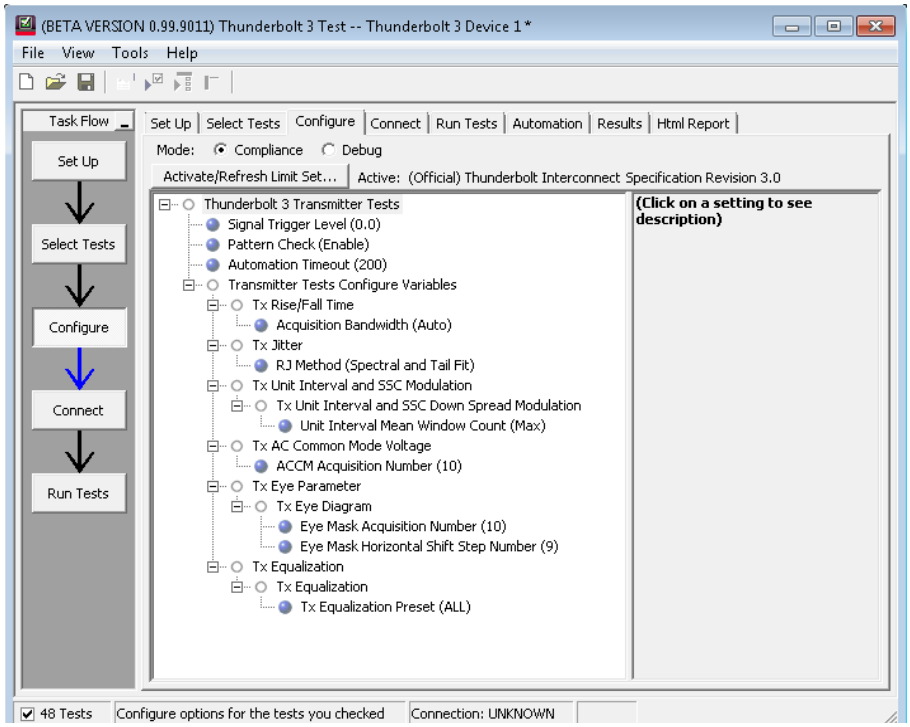


Figure 23 Configure options for Thunderbolt Tests

5 Under the **Connect** tab, the Thunderbolt Electrical Compliance Test Application displays a Connection Diagram along with a list of instructions. Figure 24 shows the connection diagram for a 2-Lane set up and Figure 25 shows the connection diagram for a 1-lane set up. If you have already set up a physical connection, you may verify else connect the DUT with the Oscilloscope as shown under this tab. Note that during some test runs, the application may prompt you for a change in physical connection/setup, as indicated in Figure 26.

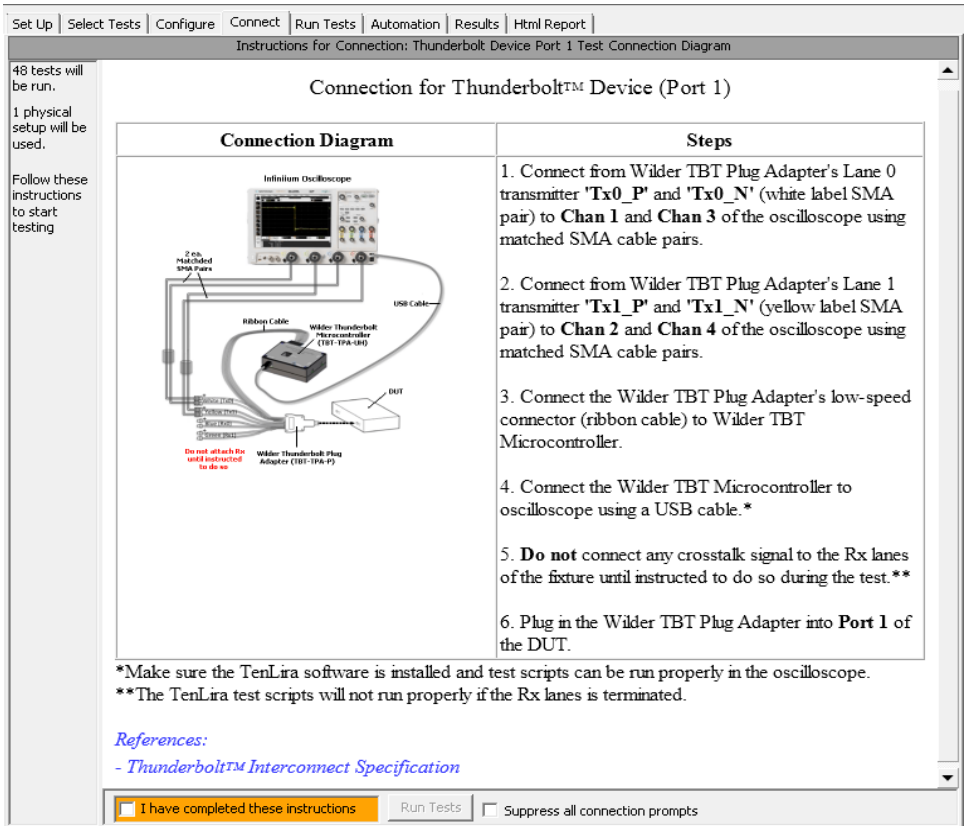


Figure 24 Connection Diagram and Instructions for a 2-Lane test set up

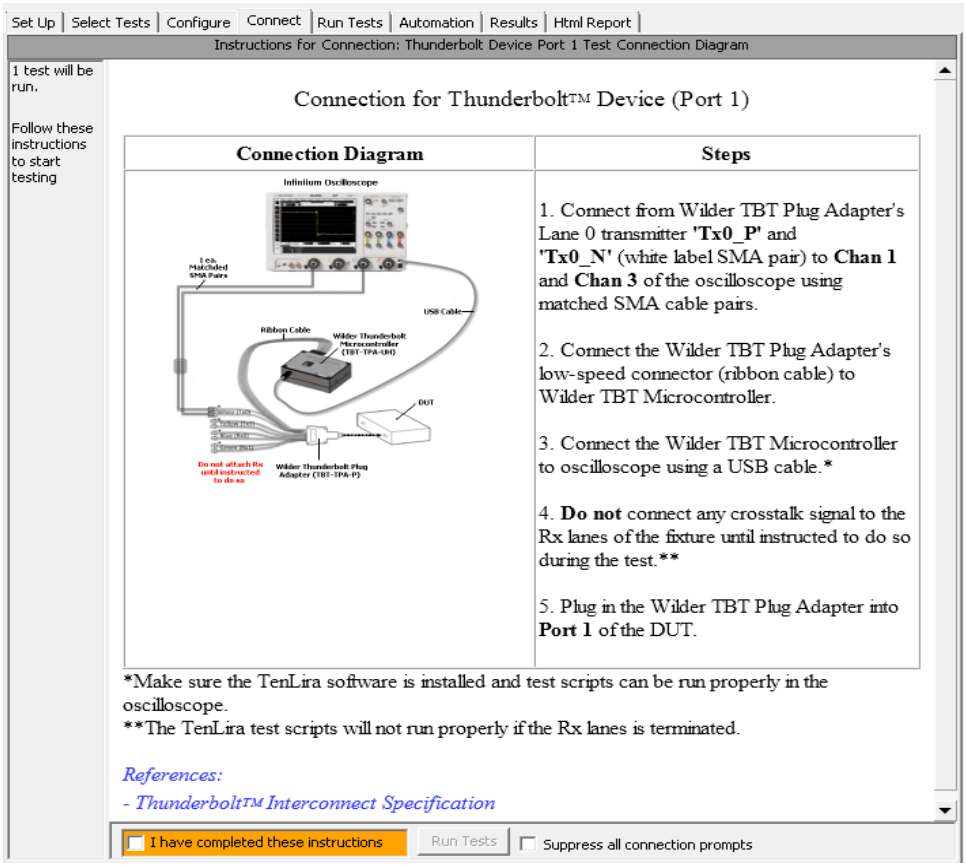


Figure 25 Connection Diagram and Instructions for a 1-Lane test set up

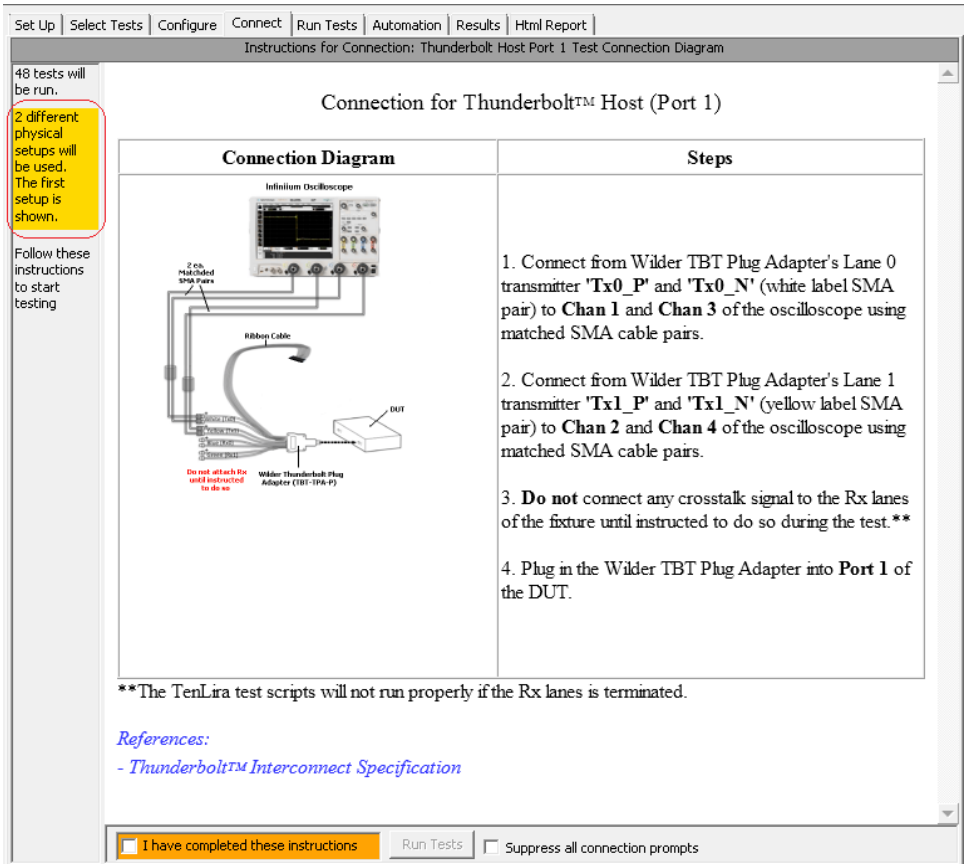


Figure 26 Indication for change of physical set up during test runs

6 Once you have performed steps 1 to 5, you are ready to run compliance tests on the Thunderbolt DUT. Additionally, you may configure/modify the run settings, automate options in the Test Application, view, export and print the test results and the HTML reports generated by the Test Application. Refer to the *Keysight N6470A Thunderbolt Electrical Compliance Test Application Online Help* to know more about how to use the Test Application.

Calibration Setup for Compliance Tests

Before running compliance tests on a Thunderbolt DUT, it is imperative that the testing equipment and its accessories be calibrated. The Thunderbolt Electrical Compliance Test Application provides the options to run Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration.

Do the following:

1 Under the **Set Up** tab of the Thunderbolt Electrical Compliance Test Application, click the **Calibrate Setup** button.

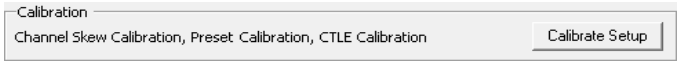


Figure 27 Calibration area under the **Set Up** tab

2 The **Calibration** window appears. It has three tabs—**Channel Skew Calibration**, **Preset Calibration** and **CTLE Calibration**. As shown in Figure 28, the **Channel Skew Calibration** tab view displays by default.

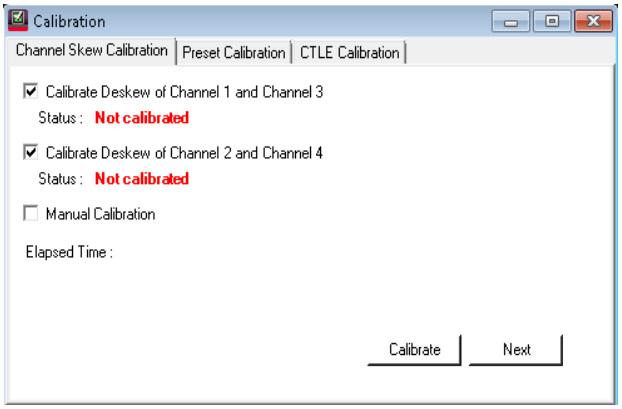


Figure 28 Default view of the **Calibration** window

Channel Skew Calibration

In order to achieve accurate test results and to verify that the Device under test is compliant to the standards, it is necessary to calibrate the Oscilloscope channels that are connected via cables to the Thunderbolt DUT.

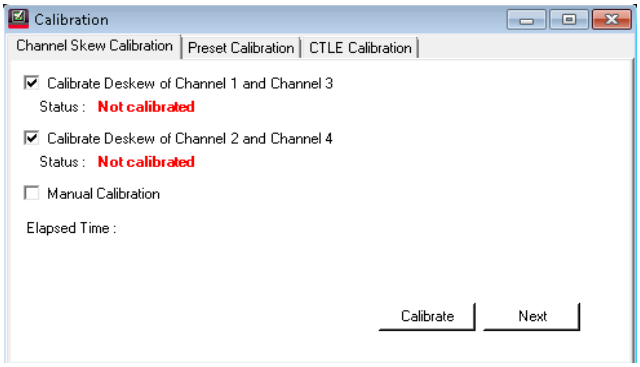


Figure 29 Channel Skew Calibration Options

Under the **Channel Skew Calibration** tab, the Thunderbolt Electrical Compliance Test Application displays the status of the Oscilloscope Channels that have been calibrated for de-skew. As shown in Figure 29, the options **Calibrate Deskew of Channel 1 and Channel 3** and **Calibrate Deskew of Channel 2 and Channel 4** are checked by default and the status of each of these options is **Not Calibrated**. You may also select the **Manual Calibration** check-box to perform Channel Skew Calibration later.

To start calibration of the selected Oscilloscope channel pairs, click the **Calibrate** button. The **Test Instruction for Thunderbolt 3 Compliance** window appears.

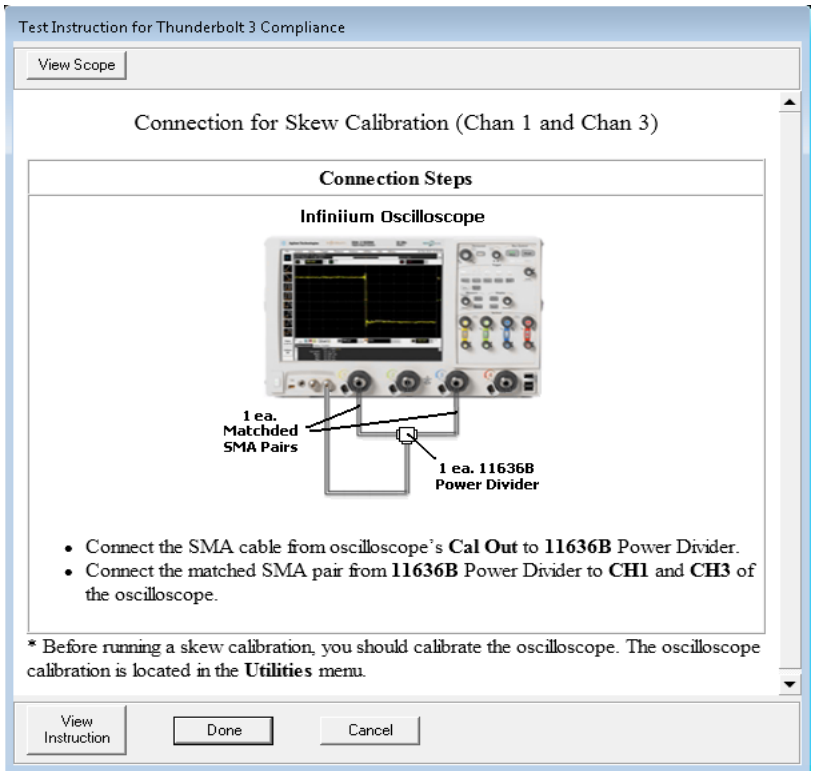


Figure 30 Instructions for Channel Skew Calibration for the selected Oscilloscope Channels

The **Test Instruction for Thunderbolt 3 Compliance** window provides instructions and connection diagram required to be set up to perform Channel Skew Calibration. Figure 30 shows the **Connection for Skew Calibration for Channel 1 and Channel 3**. Repeat these instructions for Skew Calibration for Channel 2 and Channel 4. Note that before you start performing Channel Skew Calibration, the Oscilloscope and probes must have been calibrated. If you have not already calibrated the oscilloscope and probe, see Chapter 6, "Calibrating the Infiniium Oscilloscope" to calibrate the Oscilloscope and probes.

On the **Test Instruction for Thunderbolt 3 Compliance** window,

1 Click the **View Scope** button to minimize this window and to see the Oscilloscope screen for the waveform and to use the Infiniium controls to perform Oscilloscope Calibration (if it has not been done yet).

2 Click the **View Instruction** button to maximize the window to view the instructions and the connection diagram again.

3 Once you have set up the physical connection for Channel Skew Calibration for the respective channels, click **Done** to begin Calibration. You may click **Cancel** at any point to simply return to the **Calibration** window.

4 When you click **Done**, the **Calibration** window displays again with the updated Status along with the time elapsed during this process, as shown in Figure 31:

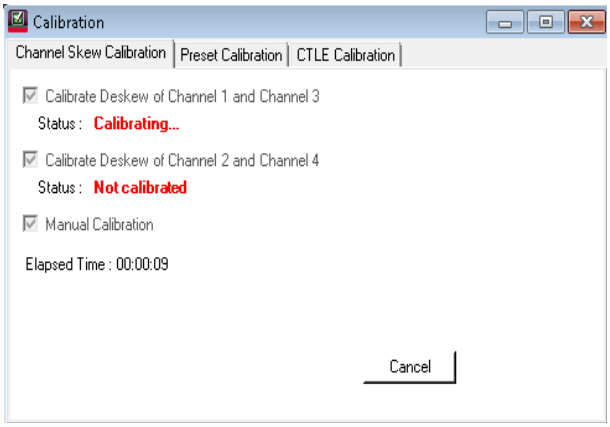


Figure 31 Calibration Status changes

Once the Calibration process is successfully done, the status changes to **Calibrated**. You may click **Cancel** to stop the process of Channel Skew Calibration at any time.

5 Before you begin Channel Skew Calibration or after the Channel Skew Calibration is complete, click the **Next** button to move to the next tab or click the tab, which you want to view.

Preset Calibration

The **Preset Calibration** tab allows you set the preset numbers on the Thunderbolt Electrical Compliance Test Application, which has been set on the Thunderbolt DUT, such that you can find the optimum preset.

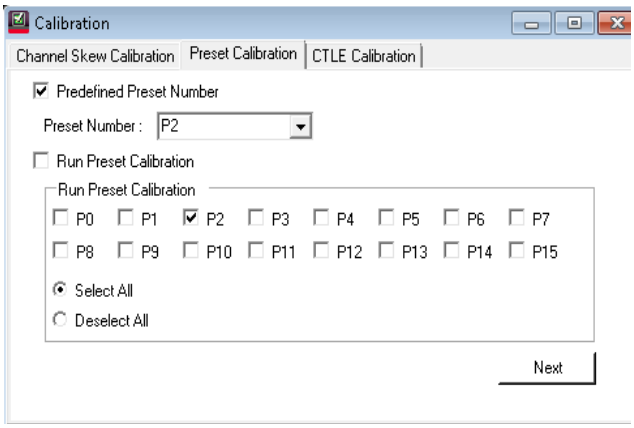


Figure 32 Default view of the Preset Calibration tab

Under the **Preset Calibration** tab,

1 By default, the **Predefined Preset Number** check-box is selected and the default Preset Number is set to **P2**.

2 From the **Preset Number :** drop-down, you may select another preset number that has been configured on the DUT.

3 Select the **Run Preset Calibration** check-box only if you wish to run Preset Calibration to find the optimum preset value for the DUT.

4 In the **Run Preset Calibration**, only **P2** is selected by default. You may select any of the preset numbers to include them for running preset calibration. You may use the **Select All** or **Deselect All** radio buttons to perform this action as well.

5 Click **Next** to move to the next tab or click the tab, which you want to view.

CTLE Calibration

The **CTLE Calibration** tab allows you set the Continuous-Time-Linear-Equalizer (CTLE) on the Thunderbolt Electrical Compliance Test Application, which has been set at the test point TP3EQ on the Thunderbolt DUT, such that you can find the optimum DC Gain value for the TP3EQ compliance tests.

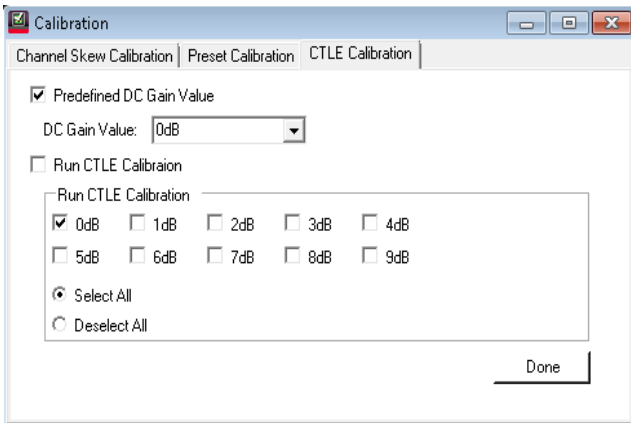


Figure 33 Default view of the CTLE Calibration tab

Under the **CTLE Calibration** tab,

1 By default, the **Predefined DC Gain Value** check-box is selected and the default DC Gain value is set to **0dB**.

2 From the **DC Gain Value:** drop-down, you may select another value for DC Gain that has been configured on the DUT.

3 Select the **Run CTLE Calibration** check-box only if you wish to run CTLE Calibration to find the optimum DC Gain value for the DUT.

4 In the **Run CTLE Calibration**, only **0dB** is selected by default. You may select any of the DC Gain values to include them for running CTLE calibration. You may use the **Select All** or **Deselect All** radio buttons to perform this action as well.

5 Click **Done** to save any modifications done to the **Calibration** window and to return to the Thunderbolt Test Environment Setup.

Tx Preset Calibration

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE **Prior to running the compliance tests, the Host / Device must go through Preset Calibration.**

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Preset Calibration* are checked.

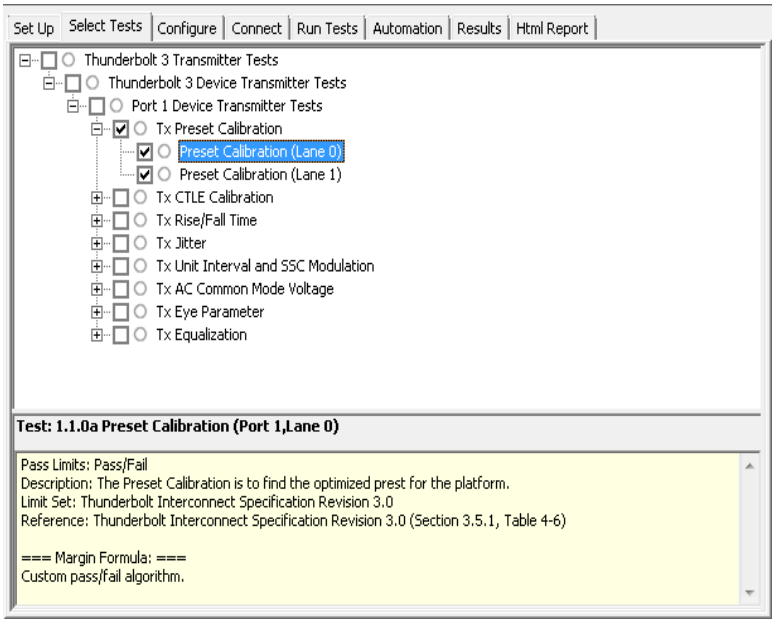


Figure 34 Selecting the Tx Preset Calibration tests

Test Procedure

1 Connect the DUT to the Oscilloscope.

2 Configure the DUT transmitter to output PRBS31, 10.3125 GB/s, Preset 0 (P0) on all lanes with SSC enabled.

3 Perform measurements with:

a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.94; no average and no interpolation to be used; set to real time eye.

b Oscilloscope with a bandwidth of 16GHz.

4 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate ≥ 50 GSa/s
   b Adjust vertical scale such that the signal fits on the Oscilloscope screen
   c Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
5 Capture eye height and eye width for lane 0.
6 Register eye height and eye width values.
7 Repeat the test for the remaining Thunderbolt lanes.
8 Repeat the test for all remaining Thunderbolt transmit presets (till preset 15 as shown in Table 5).
9 For each lane, choose the preset that provides maximum eye width. If there are two presets with the same eye width, choose the one with the greater eye height.

Expected / Observable Results

For each lane, the preset that provides the maximum eye width is the optimized preset for the platform. If two presets have the same eye width, the preset with a greater eye height is the optimized preset.

Test References

See

- "Section 3.3.1 Preset Calibration for 10.3125 Gb/s" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-5 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx CTLE Calibration

Test Overview

The objective of the Tx CTLE Calibration Test is to find the optimized CTLE (Continuous-Time-Linear-Equalizer) for the platform.

See "Reference CTLE" on page 33 to know more about CTLE.

NOTE **Apply equalization on the Oscilloscope, when testing at TP3EQ.**

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx CTLE Calibration* are checked.

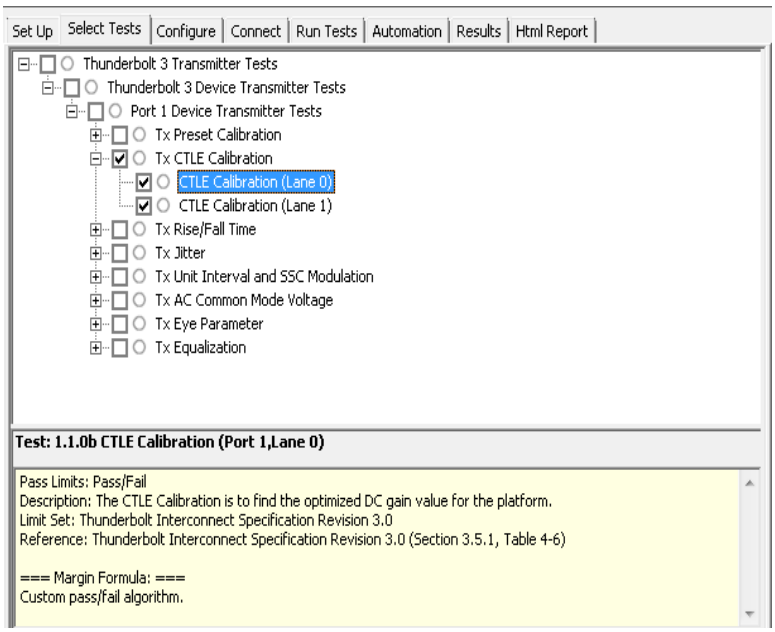


Figure 35 Selecting the Tx CTLE Calibration tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31, 10.3125 GB/s with SSC enabled.
2. Perform measurements with:
   a. 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b. Oscilloscope with a bandwidth of 16GHz
   c. Set Oscilloscope to show real time eye
3. Follow the CTLE model as described in "Reference CTLE" on page 33, with the following parameters:
   a. AC Gain – 1.41
   b. Pole 1 – 1.5 G rad/sec
   c. Pole 2 – 5 G rad/sec
4. Calibrate DC Gain using the following equation:

$$\max_{\text{DC Gain}} (\text{eye height}),\ \text{DC Gain} = \{10^{-x/20} : x = 0 \div 9\ [\text{dB}]\}$$

5. Register eye height and eye width values.
6. Repeat the test for the remaining Thunderbolt lanes.
7. For each lane, choose the DC Gain value that provides maximum eye height. If there are two DC Gain values with the same eye height, choose the one with the greater eye width.
8. After optimizing the CTLE, apply automatic DFE (Decision-Feedback-Equalizer) with a maximum tap of 50mV. See "Reference DFE" on page 35 to know more about DFE.

Expected / Observable Results

For each lane, the DC Gain value that provides the maximum eye height is the optimized CTLE for the platform. If two DC Gain values have the same eye height, the one with a greater eye width is the optimized CTLE.

Test References

See

- "Section 5. Appendix A – CTLE Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Section 5.4.4.1 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Rise/Fall Time

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the Thunderbolt differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time $\geq$ 10ps (Refer to Table 4 on page 36).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.
2. Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.
3. Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Rise/Fall Time* are checked.

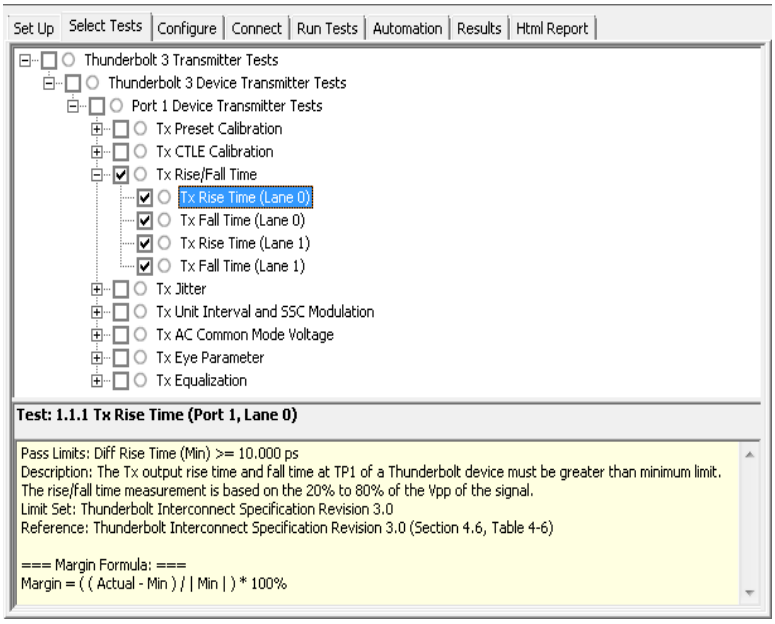


Figure 36 Selecting the Tx Rise/Fall Time tests

Test Procedure

1. Configure the DUT transmitter to output alternating square pattern of 32 0's and 32 1's on all lanes with SSC enabled.
2. Evaluate at least 4Mpts per channel (use the maximum analog bandwidth of the Oscilloscope). No CDR, no average and no interpolation to be used.
3. Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.

4 Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If T_{RISE} < 10ps, the status of test is FAIL.

If T_{FALL} < 10ps, the status of test is FAIL.

Test References

See

- "Section 3.4.8 Rise/Fall Time Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Total Jitter

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ) $\leq$ 0.38 UI_{p-p} (Refer to Table 6 on page 40).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see “Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

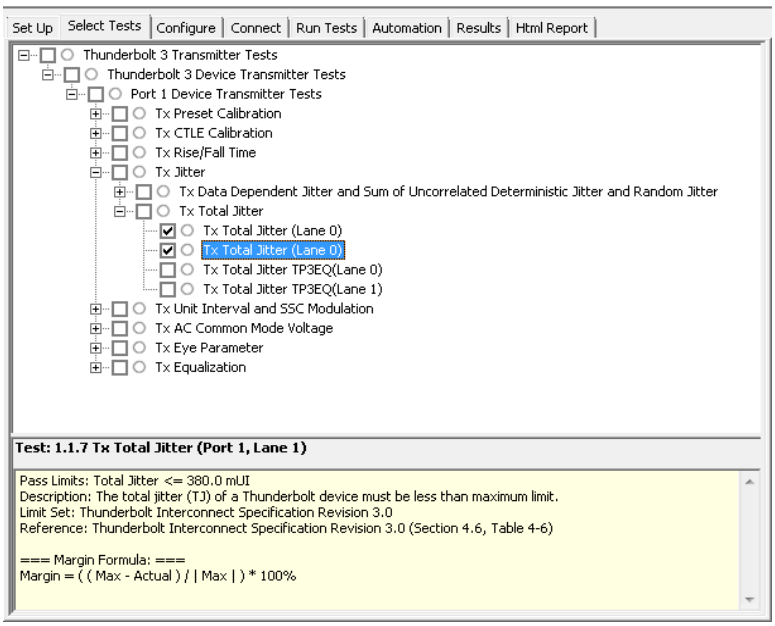


Figure 37 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Perform measurements with:

a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.94; no average and no interpolation to be used

b Oscilloscope with a bandwidth of 16GHz

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate ≥ 50 GSa/s
   b Pattern length – Arbitrary (at least -2, 11)
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 26Mpts per channel and horizontal scale of 25 µs / square

4 If TJ > 0.38 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
   b Perform measurements with:
   - 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - Oscilloscope with a bandwidth of 16GHz

   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate ≥ 50 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Adjust vertical scale such that the signal fits on the Oscilloscope screen
   - Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   - Referenced to 1E-13 statistics
   - Capture the Deterministic Jitter (DJ) result

   d Configure the DUT transmitter to output alternating square pattern of 1 0's and 1 1's (square pattern) on all lanes with SSC enabled.
   e Perform measurements with:
   - 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - Oscilloscope with a bandwidth of 16GHz

   f Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate ≥ 50 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Adjust vertical scale such that the signal fits on the Oscilloscope screen
   - Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   - Referenced to 1E-13 statistics
   - Capture the Random Jitter (RJ) result

   g Calculate TJ using the equation:

$$TJ = DJ + 14.7 * RJ$$

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If TJ > 0.38 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.9 Total Jitter" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Sum of Uncorrelated Jitter

Test Overview

The objective of the Tx Sum of Uncorrelated Jitter Test is to confirm that the sum of Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Sum of Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 6 on page 40).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Data Dependent Jitter and Sum of Uncorrelated Deterministic Jitter and Random Jitter* are checked.

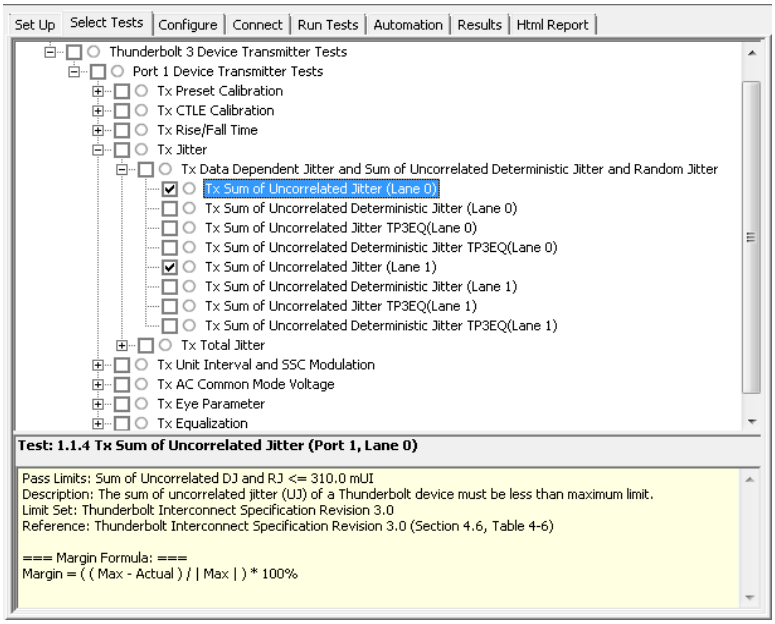


Figure 38 Selecting the Tx Sum of Uncorrelated Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.

2 Perform measurements with:

a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.94; no average and no interpolation to be used

b Oscilloscope with a bandwidth of 16GHz

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 50 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits on the Oscilloscope screen
   e Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   f Referenced to 1E-13 statistics
4 Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5 Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.10 UJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Sum of Uncorrelated Deterministic Jitter

Test Overview

The objective of the Tx Sum of Uncorrelated Deterministic Jitter Test is to confirm that the sum of Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Sum of Uncorrelated Deterministic Jitter (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 6 on page 40).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Data Dependent Jitter and Sum of Uncorrelated Deterministic Jitter and Random Jitter* are checked.

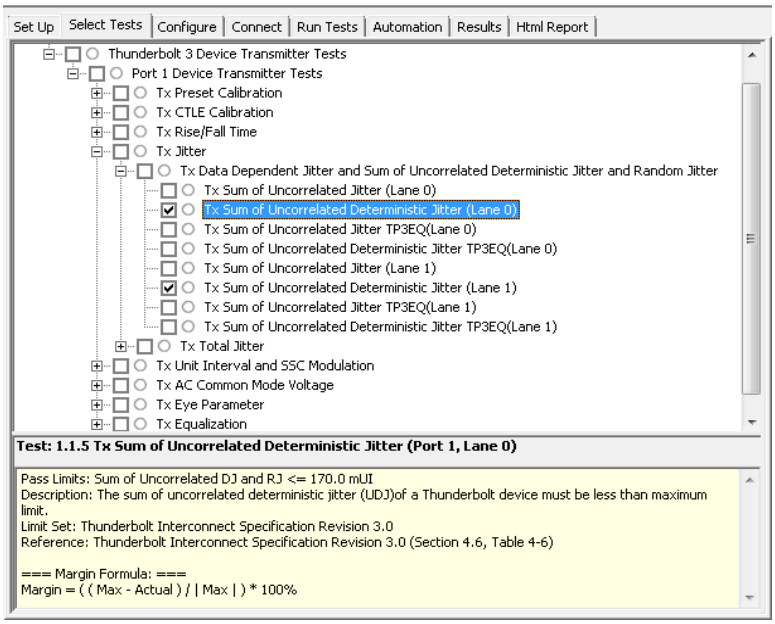


Figure 39 Selecting the Tx Sum of Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.

2 Perform measurements with:

a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.94; no average and no interpolation to be used

b Oscilloscope with a bandwidth of 16GHz

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate ≥ 50 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits on the Oscilloscope screen
   e Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   f Referenced to 1E-13 statistics
4 Capture the BUJ result.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.11 UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Unit Interval

Test Overview

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

96.9406ps ≤ Unit Interval ≤ 97.4864ps (Refer to Table 6 on page 40).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

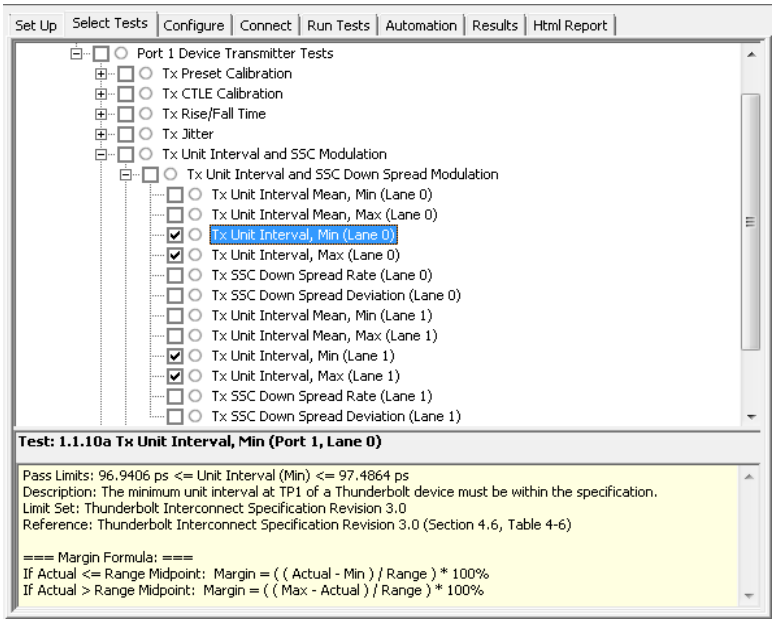


Figure 40 Selecting the Tx Unit Interval tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 26Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 16GHz

3 Calculate UI dynamically using the moving average procedure with a window size of 3000 symbols. Measure the values of both UI_{MAX} and UI_{MIN}.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UI_{MAX} > 97.4864ps, the status of test is FAIL.

If UI_{MIN} < 96.9406ps, the status of test is FAIL.

Test References

See

- "Section 3.4.2 Unit Interval Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Unit Interval Mean

Test Overview

The objective of the Tx Unit Interval Mean Test is to confirm that the average data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

97.1835ps ≤ Average Unit Interval ≤ 97.2419ps (Refer to Table 6 on page 40).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

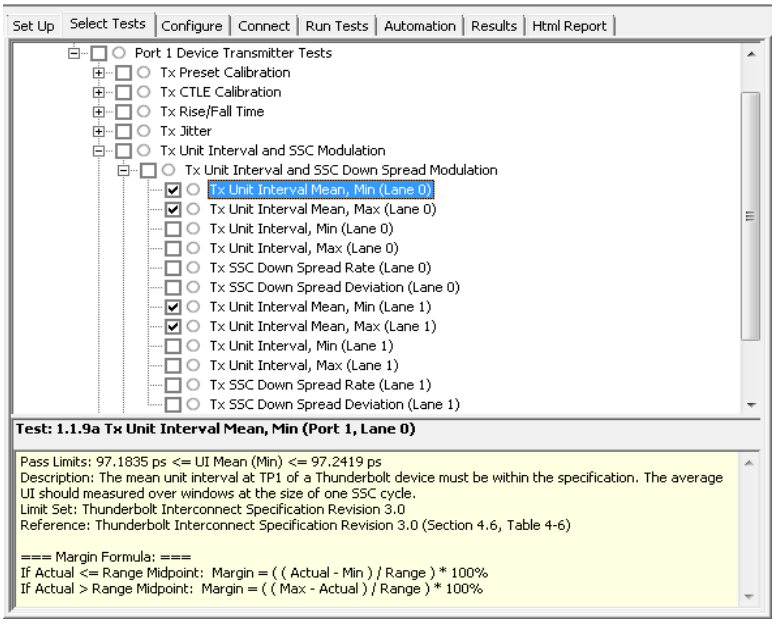


Figure 41 Selecting the Tx Unit Interval Mean tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 26Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 16GHz

3 Use mathematical analysis to measure the average unit interval over window at the size of one SSC cycle, determined by the SSC_Down_Spread_Rate.

4 Measure UI_MEAN over different windows that uniformly cover the scope capture over at least 300ms (more than 10 SSC Cycles) with 10000 UI window jumps. See Figure 42.

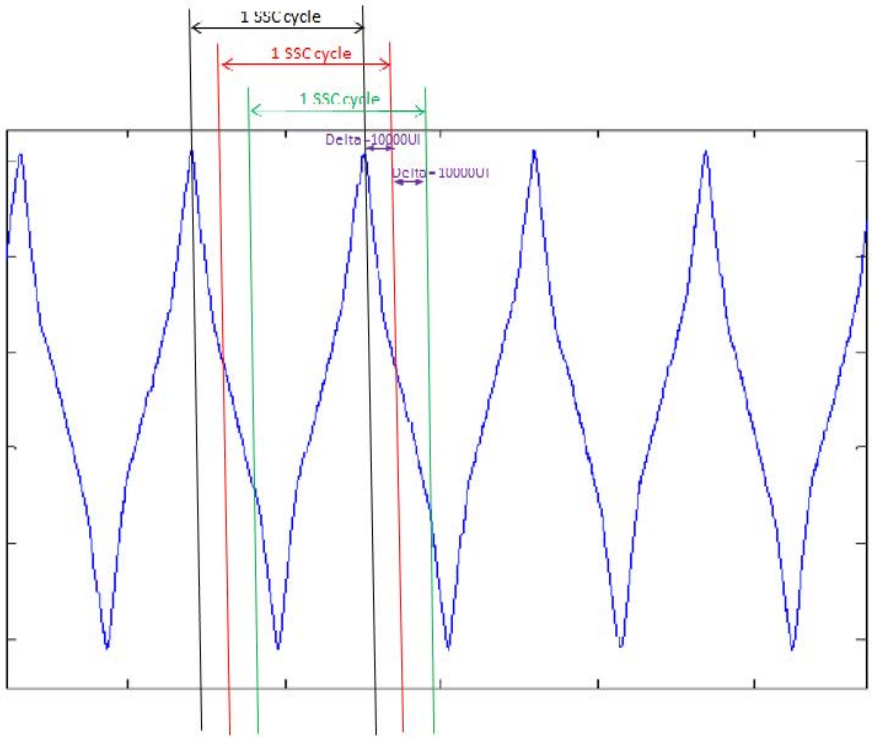


Figure 42 Measurement of UI_MEAN over at least 10 SSC Cycles

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the maximum UI_MEAN measured > 97.2419ps, the status of test is FAIL.

If the minimum UI_MEAN measured < 97.1835ps, the status of test is FAIL.

Test References

See

- "Section 3.4.3 Unit Interval Mean Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx SSC Down Spread Deviation

Test Overview

The objective of the Tx SSC Down Spread Deviation Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

-0.03% ≤ SSC_Down_Spread_Deviation ≤ 0.53% (Refer to Table 4 on page 36).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

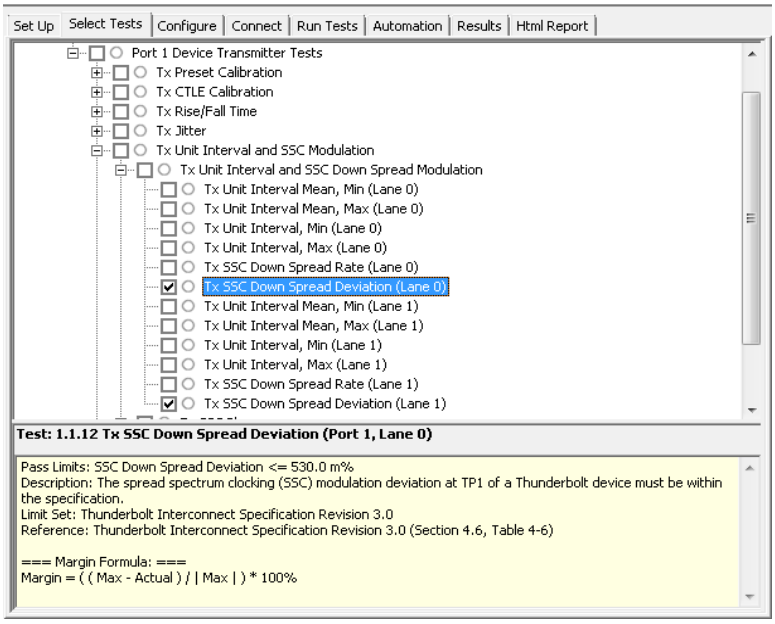


Figure 43 Selecting the Tx SSC Down Spread Deviation tests

Test Procedure

1 Run the "Tx Unit Interval" Test as a prerequisite to obtain UI_{MAX}.

2 Use the obtained value of UI_{MAX} to calculate the Deviation percentage:

$$Deviation = 100*\{[(1 / UI_{MAX}) - 10.3125GB/s] / 10.3125GB/s\}$$

Expected / Observable Results

If SSC_Down_Spread_Deviation > 0.53% or SSC_Down_Spread_Deviation < -0.03%, the status of test is FAIL.

Test References

See

- “Section 3.4.4 SSC Down Spread Deviation Measurements” of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5.*

Tx SSC Down Spread Rate

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

35KHz ≤ SSC_Down_Spread_Rate ≤ 37KHz (Refer to Table 4 on page 36).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

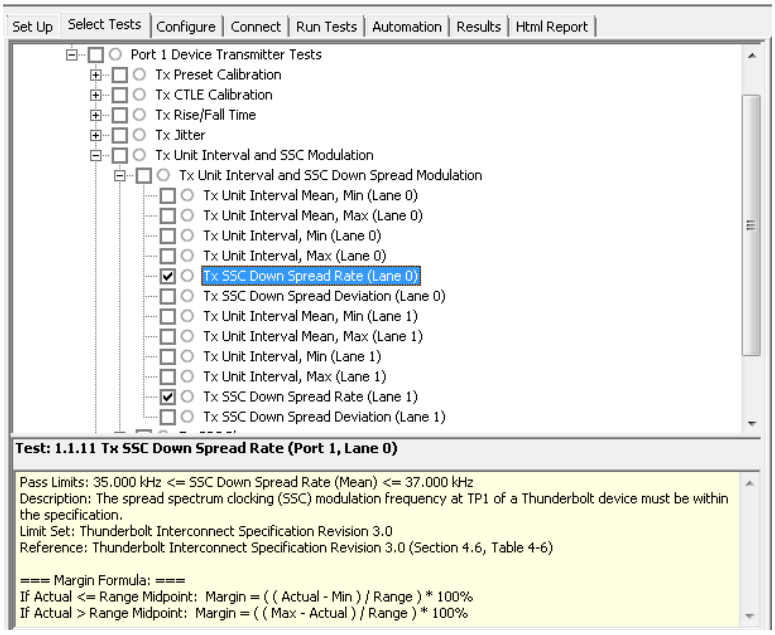


Figure 44 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 26Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 16GHz

3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If 35KHz > SSC_Down_Spread_Rate > 37KHz, the status of test is FAIL.

Test References

See

- "Section 3.4.5 SSC Down Spread Rate Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5.*

Tx SSC Phase Deviation

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.5ns p-p ≤ SSC_Phase_Deviation ≤ 16.5ns p-p (Refer to Table 4 on page 36).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx SSC Phase* are checked.

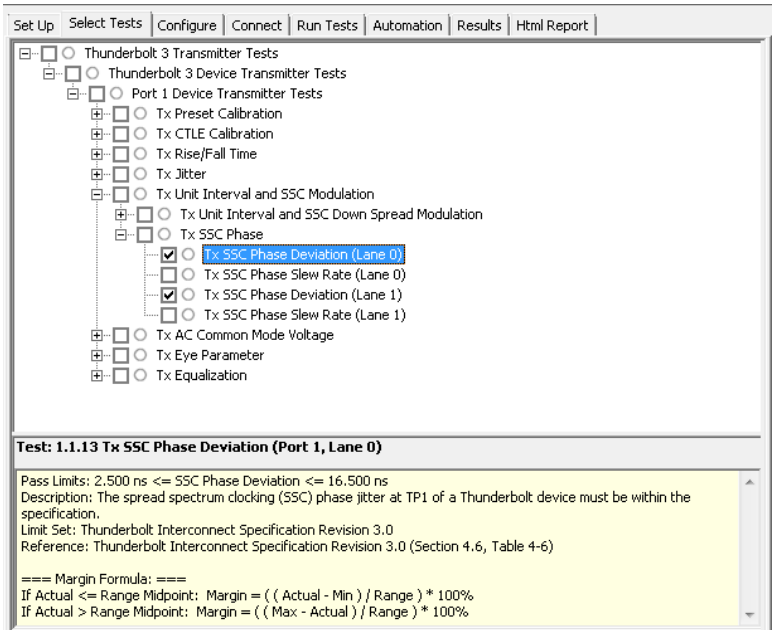


Figure 45 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and post process it with an appropriate software:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 40Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 16GHz

3 Extract the SSC Phase Deviation from the transmitted signal. The SSC Phase Deviation should be extracted from the phase jitter after applying a 2nd order low-pass filter with 3dB point at 5 MHz, damping factor 0.94.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If 2.5ns p-p > SSC_Phase_Deviation > 16.5ns p-p, the status of test is FAIL.

Test References

See

- "Section 3.4.6 SSC Phase Deviation Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx SSC Phase Slew Rate

Test Overview

The objective of the Tx SSC Phase Slew Rate Test is to confirm that the SSC Phase Jitter Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Phase_Slew_Rate ≤ 3.3ms/s (Refer to Table 4 on page 36).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx SSC Phase* are checked.

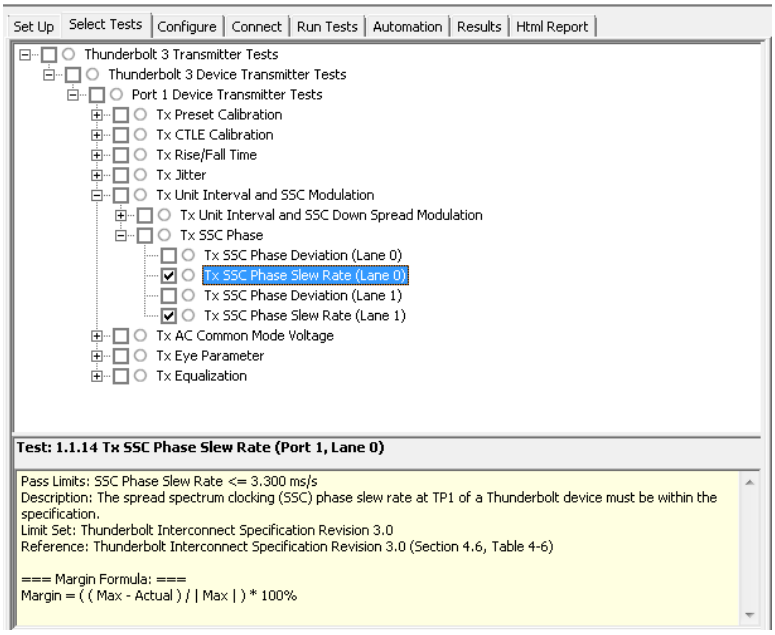


Figure 46 Selecting the Tx SSC Phase Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and post process it with an appropriate software:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 40Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 16GHz

3 Extract the SSC Phase Slew Rate from the transmitted signal. The SSC Slew Rate should be extracted from the phase jitter after applying a 2nd order low-pass filter with 3dB point at 5 MHz, damping factor 0.94.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Phase_Slew_Rate > 3.3ms/s, the status of test is FAIL.

Test References

See

- "Section 3.4.7 SSC Phase Slew Rate Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Eye Diagram

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 47.

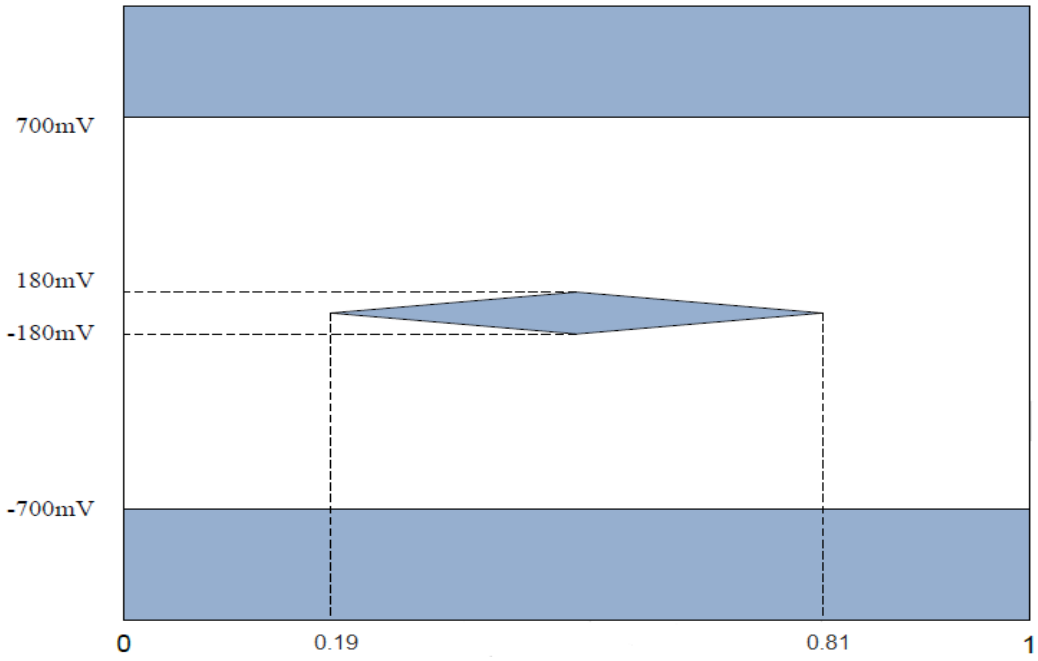


Figure 47 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 6 on page 40 and Figure 17 on page 42).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

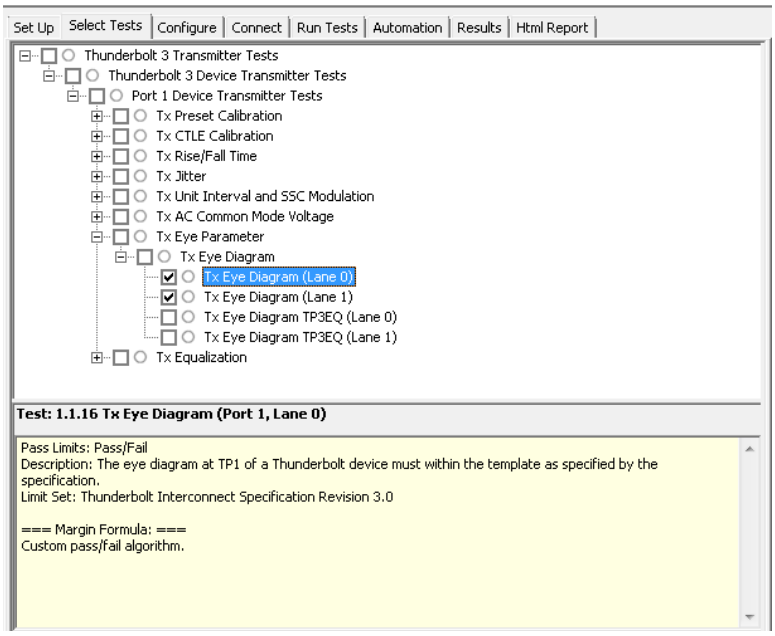


Figure 48 Selecting the Tx Eye Diagram tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate $\geq$ 50 GSa/s

b Perform measurements with a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5MHz and damping factor of 0.94. No average and no interpolation to be used. Oscilloscope must have a bandwidth of 16GHz

c Accumulate at least 1E6 bits, adjust the memory depth and test duration in order to obtain at least 10 waveforms

3 Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section “Expected / Observable Results”.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/- 700mV), the status of the test is FAIL.

ii Shift the mask left or right through one entire T_{BIT} to determine if any horizontal position has no capture points within the eye mask. No vertical shifting of the mask is allowed.

iii If no such shifted position exists where no part of the waveform touches or crosses into the data eye, the status of the test is FAIL.

Test References

See

- "Section 3.4.12 Eye Diagram Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-6 and Figure 5-11 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx AC Common Mode Voltage

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the Thunderbolt differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq 100mV_{p-p}$ (Refer to Table 6 on page 40).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx AC Common Mode Voltage* are checked.

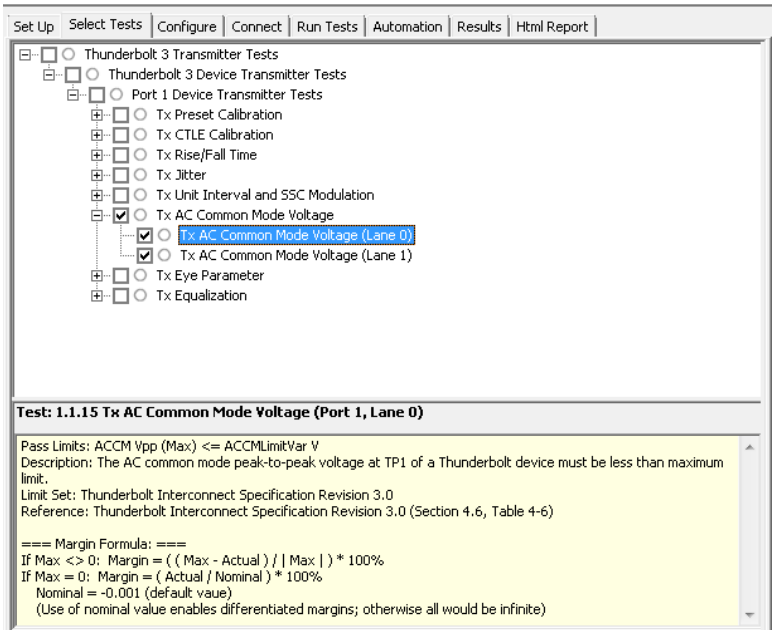


Figure 49 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 50 GSa/s
   b Evaluate 26Mpts per channel
   c Set vertical scale to 20mV/Div
   d No CDR, no average and no interpolation to be used
   e Oscilloscope must have a bandwidth of 16GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $V_{AC-CM} > 100mV_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.13 AC Common Mode Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-6 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Equalization Tests

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Pre-shoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Pre-shoot, De-Emphasis: ± 1dB for the following presets:

Table 10 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.7
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	4.3	-9.3
15	1.7	-1.7

(Refer to Table 5 on page 38).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Equalization* are checked.

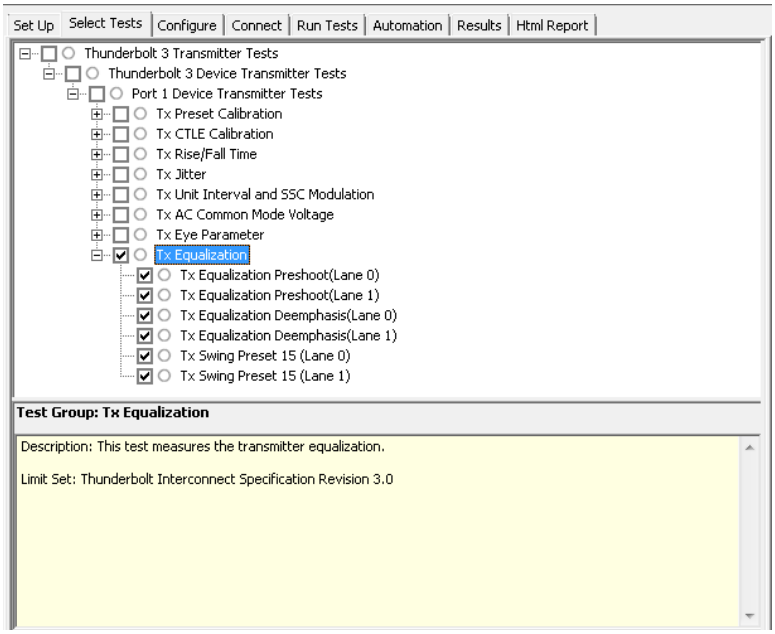


Figure 50 Selecting the Tx Equalization tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the Configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

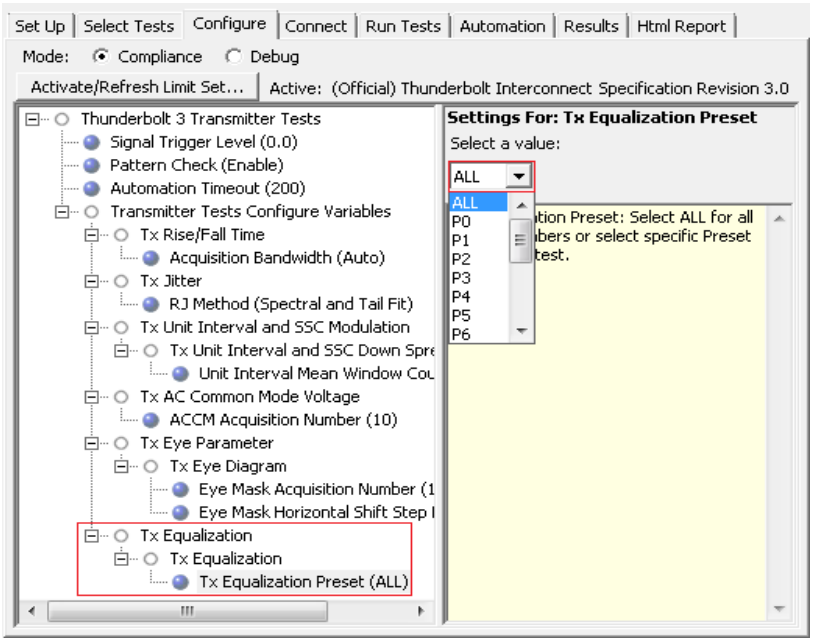


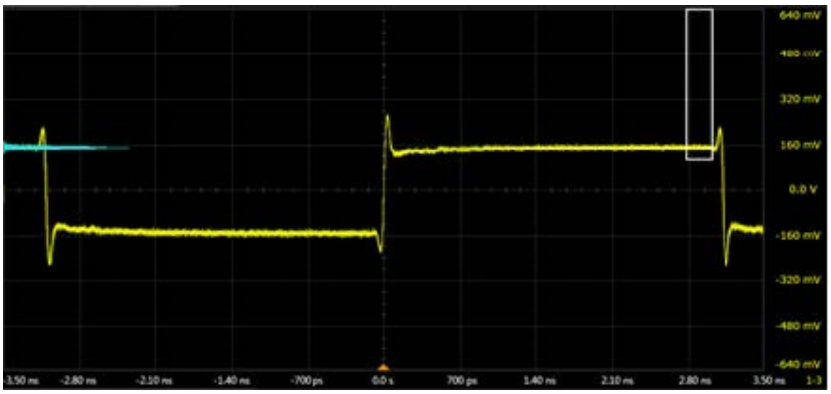
Figure 51 Configuring Tx Equalization Preset Variable

Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 16GHz.

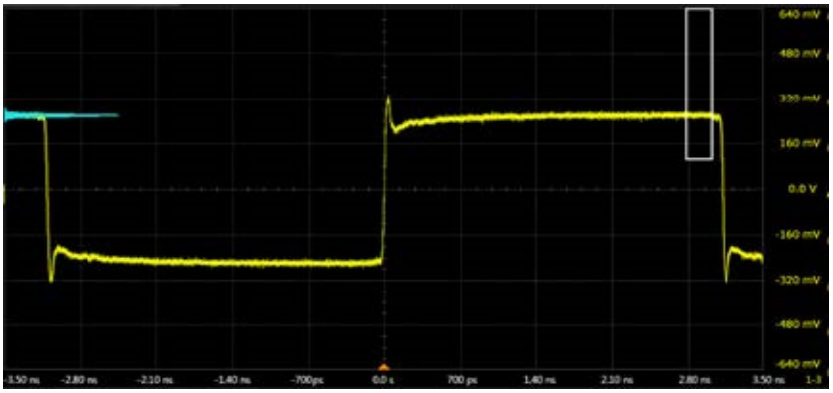


4 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

5 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

6 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 16GHz.

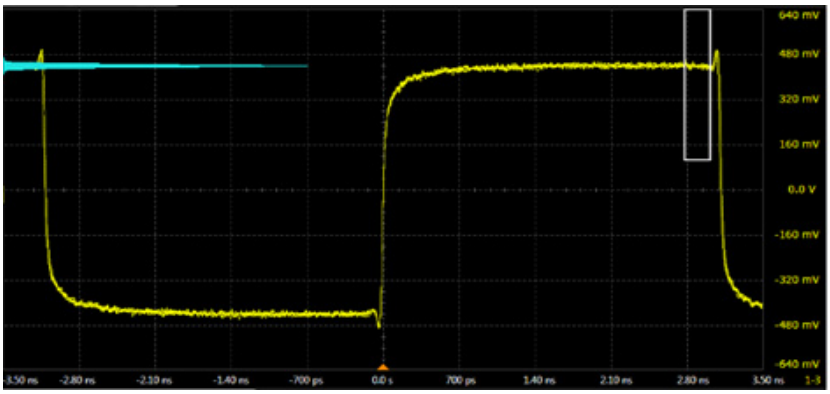


7 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

8 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

9 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 16GHz.



10 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Pre-Shoot to be } 20 * \log_{10} [V_2/V_1]$$

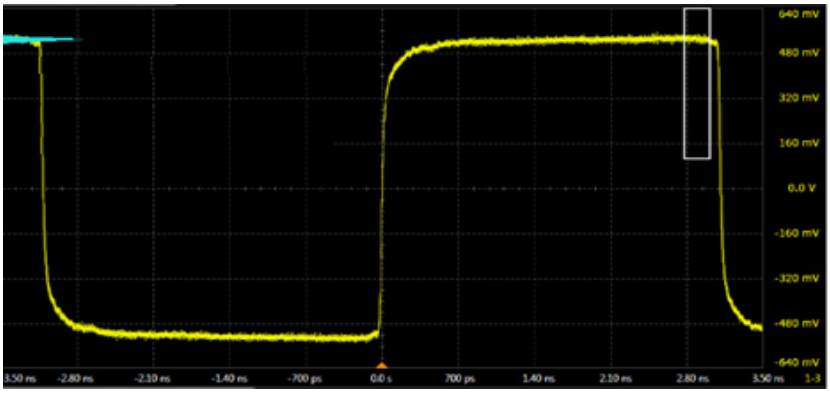
$$\text{Set De-Emphasis to be } 20 * \log_{10} [V_1/V_3]$$

11 Repeat steps 2 to 10 for all Presets defined in Table 10.

12 Set the DUT to Preset 0 (P0).

13 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

14 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 16GHz.



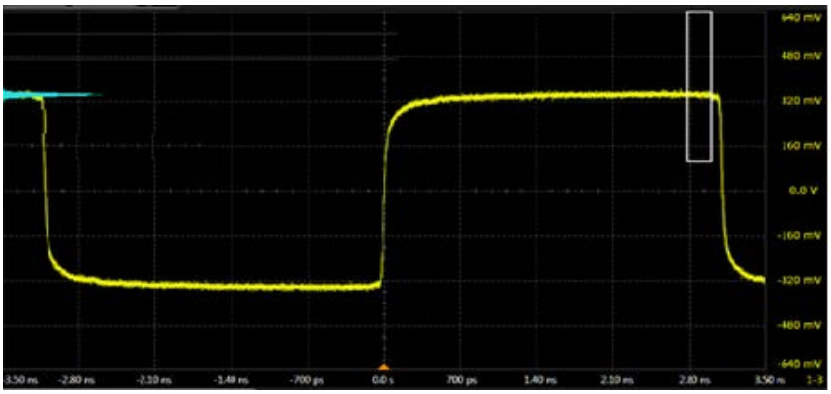
15 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

$$V_0 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

16 Set the DUT to Preset 15 (P15).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 16GHz.



19 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Swing to be } 20 * \log_{10} [V_0/V_{15}]$$

20 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 10, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 10, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- "Section 3.4.1 Transmitter Equalization" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-5 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Total Jitter TP3EQ

Test Overview

The objective of the Tx Total Jitter TP3EQ Test is to confirm that the Total Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ_{TP3EQ}) ≤ 0.66 UI_{p-p} (Refer to Table 7 on page 41).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see “Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

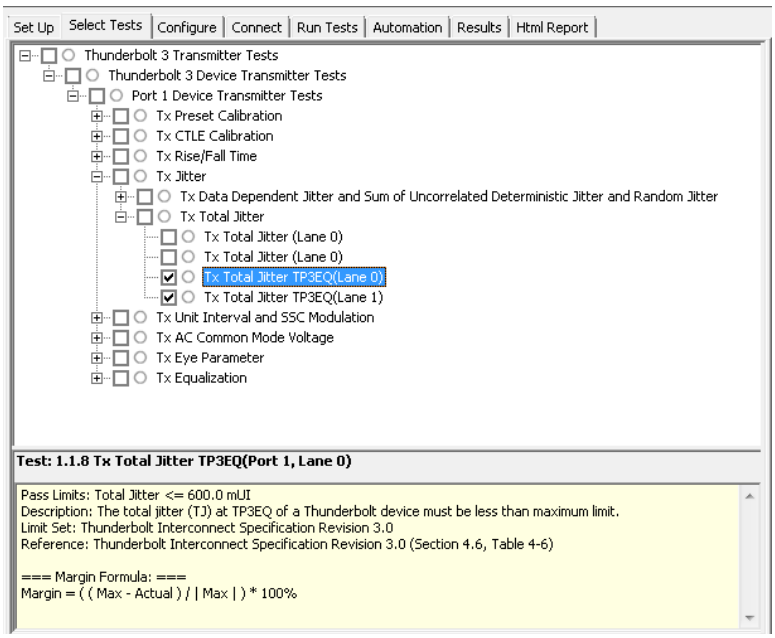


Figure 52 Selecting the Tx Total Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Ensure that measurements are done with a calibrated CTLE. See “Tx CTLE Calibration" on page 61.

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate ≥ 50 GSa/s
   b Pattern length – Arbitrary (at least -2, 11)
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
4 If TJ > 0.66 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
   b Ensure that measurements are done with a calibrated CTLE. See "Tx CTLE Calibration" on page 61.
   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate ≥ 50 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Adjust vertical scale such that the signal fits on the Oscilloscope screen
   - Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   - Referenced to 1E-13 statistics
   - Capture the Deterministic Jitter (DJ_{TP3EQ}) result

   d Configure the DUT transmitter to output alternating square pattern of 1 0's and 1 1's (square pattern) on all lanes with SSC enabled.
   e Perform measurements with:
   - 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.94; no average and no interpolation to be used

   f Ensure that measurements are done with a calibrated CTLE. See "Tx CTLE Calibration" on page 61.
   g Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate ≥ 50 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Adjust vertical scale such that the signal fits on the Oscilloscope screen
   - Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   - Referenced to 1E-13 statistics
   - Capture the Random Jitter (RJ_{TP3EQ}) result

   h Calculate TJ_{TP3EQ} using the equation:

$$TJ_{TP3EQ} = DJ_{TP3EQ} + 14.7 * RJ_{TP3EQ}$$

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If TJ_{TP3EQ} > 0.66 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.4.14 Total Jitter TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-7 of the *Thunderbolt Interconnect Specification Rev 1.5.*

Tx Sum of Uncorrelated Jitter TP3EQ

Test Overview

The objective of the Tx Sum of Uncorrelated Jitter TP3EQ Test is to confirm that the sum of Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Sum of Uncorrelated Jitter (UJ_{TP3EQ}) ≤ 0.33 UI_{p-p} (Refer to Table 7 on page 41).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Data Dependent Jitter and Sum of Uncorrelated Deterministic Jitter and Random Jitter* are checked.

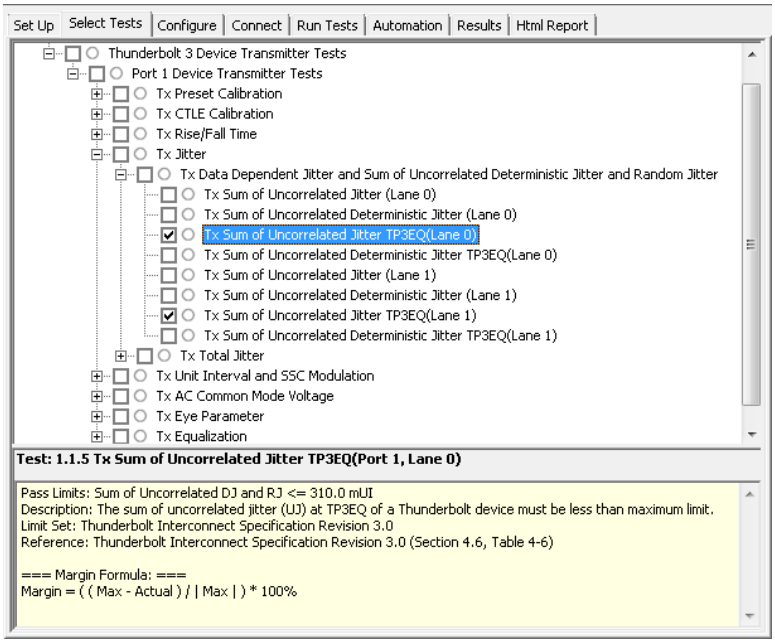


Figure 53 Selecting the Tx Sum of Uncorrelated Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.

2 Ensure that measurements are done with a calibrated CTLE. See "Tx CTLE Calibration" on page 61.

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 50 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits on the Oscilloscope screen
   e Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   f Referenced to 1E-13 statistics
4 Capture the Total Jitter (TJ_{TP3EQ}) and Data Dependent Jitter (DDJ_{TP3EQ}) results.
5 Calculate UJ_{TP3EQ} using the equation:

$$UJ_{TP3EQ} = TJ_{TP3EQ} - DDJ_{TP3EQ}$$

6 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UJ_{TP3EQ} > 0.33\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.15 UJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-7 of the *Thunderbolt Interconnect Specification Rev 1.5.*

Tx Sum of Uncorrelated Deterministic Jitter TP3EQ

Test Overview

The objective of the Tx Sum of Uncorrelated Deterministic Jitter TP3EQ Test is to confirm that the sum of Uncorrelated Deterministic Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Sum of Uncorrelated Deterministic Jitter (UDJ_{TP3EQ}) ≤ 0.17 UI_{p-p} (Refer to Table 7 on page 41).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.
2. Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.
3. Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Data Dependent Jitter and Sum of Uncorrelated Deterministic Jitter and Random Jitter* are checked.

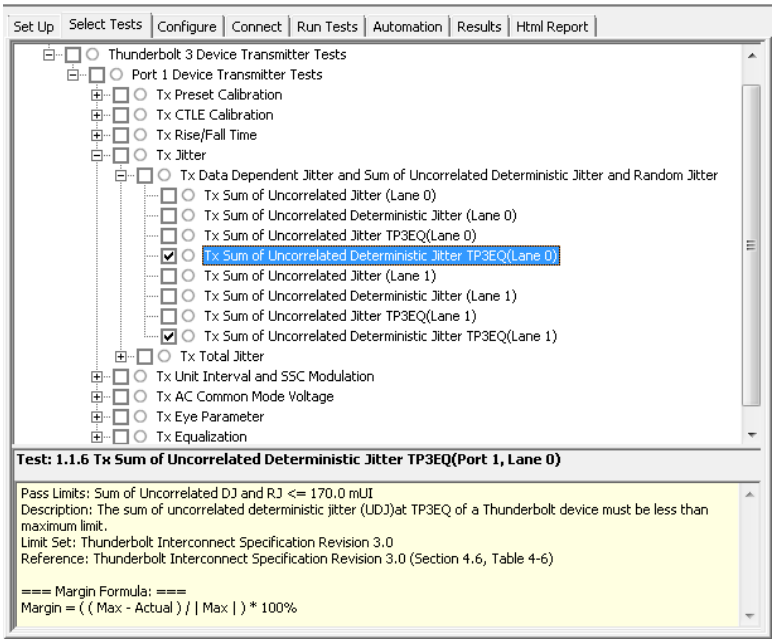


Figure 54 Selecting the Tx Sum of Uncorrelated Deterministic Jitter TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Ensure that measurements are done with a calibrated CTLE. See "Tx CTLE Calibration" on page 61.

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 50 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits on the Oscilloscope screen
   e Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   f Referenced to 1E-13 statistics
4 Capture the BUJ result.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UDJ_{TP3EQ} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.4.16 UDJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-7 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Eye Diagram TP3EQ

Test Overview

The objective of the Tx Eye Diagram TP3EQ Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3EQ should meet the conditions depicted in Figure 55.

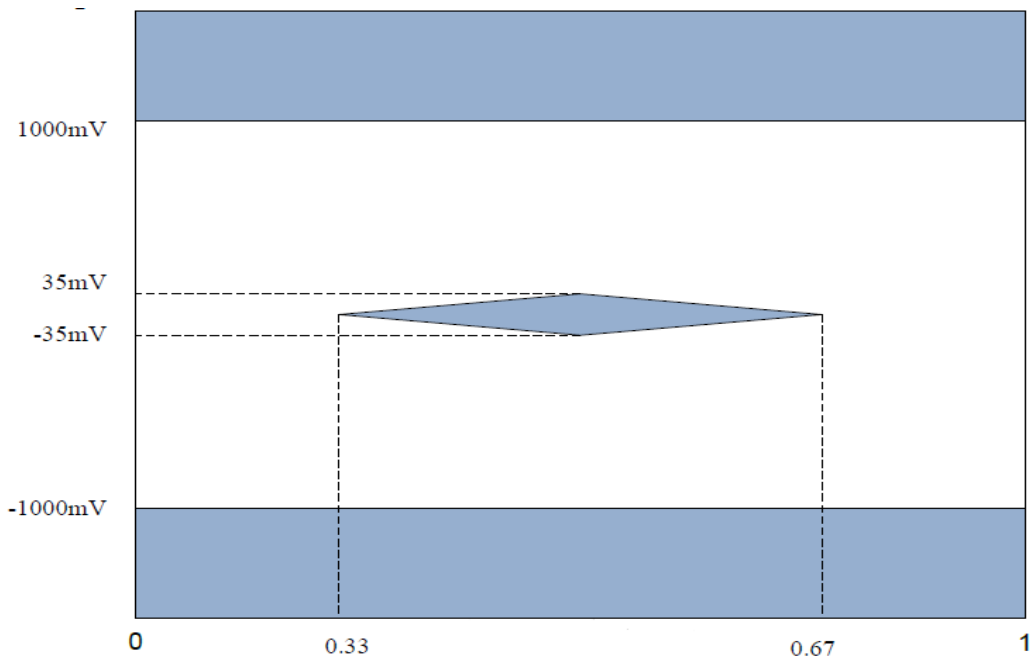


Figure 55 Pass Condition for Tx Eye Diagram TP3EQ Tests

(Refer to Table 7 on page 41 and Figure 17 on page 42).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 10.3125 GB/s Systems" on page 48.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 55.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

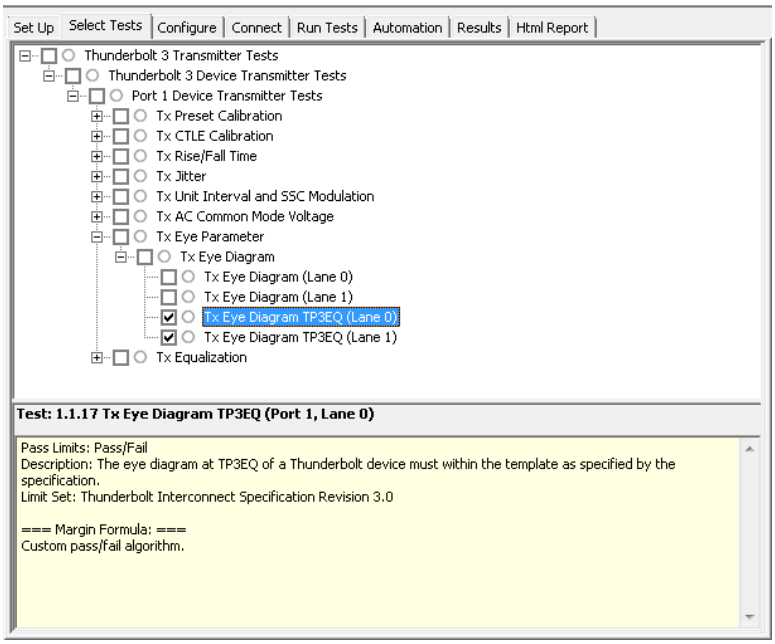


Figure 56 Selecting the Tx Eye Diagram TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 50 GSa/s

b Ensure that measurements are done with a calibrated CTLE. See "Tx CTLE Calibration" on page 61.

c Accumulate at least 1E6 bits, adjust the memory depth and test duration in order to obtain at least 10 waveforms

3 Compare the data eye to the TP3EQ eye diagram mask. Check for conditions described in the section “Expected / Observable Results”.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/-1000mV), the status of the test is FAIL.

ii Shift the mask left or right through one entire T_{BIT} to determine if any horizontal position has no capture points within the eye mask. No vertical shifting of the mask is allowed.

iii If no such shifted position exists where no part of the waveform touches or crosses into the data eye, the status of the test is FAIL.

Test References

See

- “Section 3.4.17 Eye Diagram Measurement TP3EQ” of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-7 and Figure 5-11 of the *Thunderbolt Interconnect Specification Rev 1.5*.

5 Transmitter Tests for 20.625 GB/s Systems

This section provides the Methods of Implementation (MOIs) to run electrical tests on a Thunderbolt DUT operating at a bit rate of 20.625 GB/s using an Keysight Infiniium Oscilloscope and other accessories, along with the Thunderbolt 3 Electrical Compliance Test Application.

Setting Up Test Application for 20.625 GB/s Systems

In order to run the electrical compliance tests on a Thunderbolt DUT operating at a bit rate of 20.625GB/s, you must set up the Thunderbolt Electrical Compliance Test Application to be able to view and select the required tests. To set up the Thunderbolt Electrical Compliance Test Application:

1 Start the Thunderbolt Electrical Compliance Test Application. See "Starting the Thunderbolt 3 Electrical Compliance Test Application" on page 23.

2 Under the **Set Up** tab, select the following options, as shown in Figure 57 and Figure 58.

a **Specification Version** – Select **Specification Rev 3.0** from the drop-down. Currently, the Test Application supports only this version.

b **Bit Rate** – Select **20.625GB/s**.

c **Device Type:** – Select DUT Type as either **Device** (default) or **Host**.

d **Number of Port:** – Select **1 Port (default)** or **2 Ports**. This drop-down field allows you to type a custom name for the ports being used for testing.

e **Test Lane:** – From the drop-down options, select either **Both Lanes** (default), **Lane 0 only** or **Lane 1 only**; depending on the number of lanes being used for testing.

f **Product Info** – Helps you in proper identification of the DUT on HTML reports. This option is particularly useful when running compliance tests on multiple DUTs.

- **Device Identifier :** – Type an appropriate name/identifier for the DUT, which is being tested. The entries are saved such that you may select the values again later, if required.
- **User Description :** – Type an appropriate description for the DUT, which is being tested. The entries are saved such that you may select the values again later, if required.
- **Comments :** – Type appropriate comments, if required.

g **Calibration** – Click the **Calibrate Setup** button to perform **Channel Skew Calibration** and if required, perform either **Preset Calibration** or **CTLE Calibration** or both, before running the respective tests.

- **Channel Skew Calibration** – Required to calibrate Channel Skew on the Oscilloscope Channels where the DUT is connected.
- **Preset Calibration** – Required to run the Transmitter Preset Calibration tests.
- **CTLE Calibration** – Required to run the Transmitter CTLE Calibration and Transmitter Equalization tests.

  See "Calibration Setup for Compliance Tests" on page 111 for more information on these calibration options.

h **Automation** – This feature is enabled only when you select **Device Type :** as **Host**. Use this feature for remote configuration and controlling of a Thunderbolt Host, which is a usually a remote PC or a Thunderbolt Micro-Controller.

For more information about using this feature, refer to "Automation" under the section "Setting Up the Test Environment" in the *Keysight N6470A Thunderbolt 3 Compliance Test Application Online Help*.

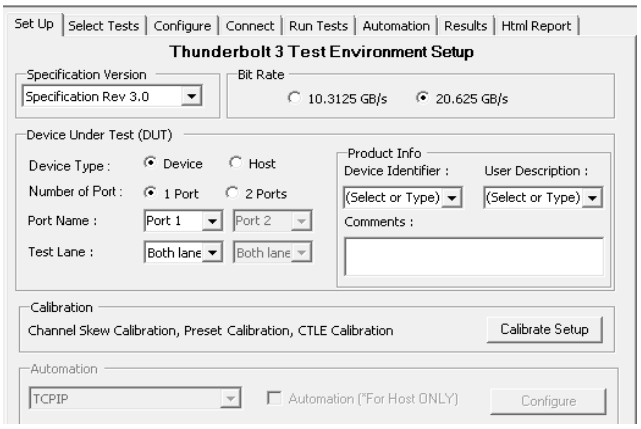


Figure 57 Set Up options for DUT Type “Device” operating at 20.625 GB/s

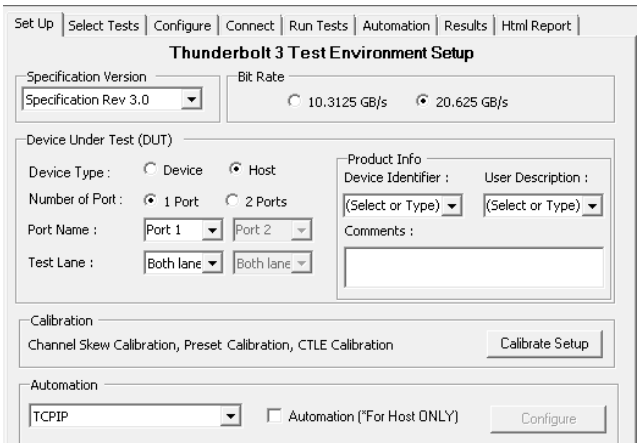


Figure 58 Set Up options for DUT Type “Host” operating at 20.625 GB/s

3 Based on your choices under the **Set Up** tab, the **Select Tests** tab displays the associated tests. For example, Figure 59 shows the compliance tests for DUT Type “Device” with 1-Port, 2-Lane system and Figure 60 shows the compliance tests for DUT Type “Host” with 1-Port, 2-Lane system. Select the tests that you want to run using the Thunderbolt Electrical Compliance Test Application. Refer to the *Keysight N6470A Thunderbolt Electrical Compliance Test Application Online Help* to know more about how to select tests.

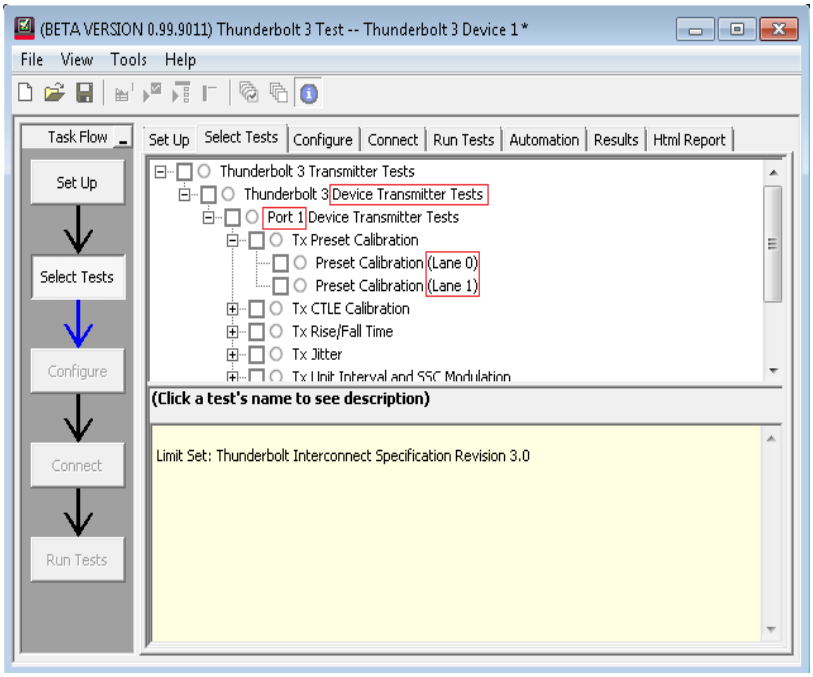


Figure 59 Select Transmitter Tests for DUT Type “Device” on 1-Port, 2-Lanes

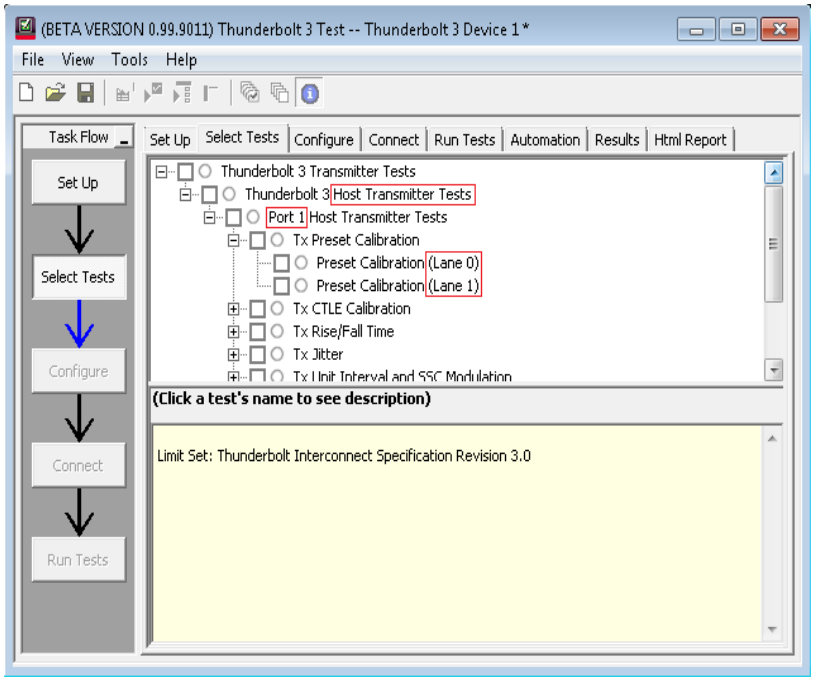


Figure 60 Select Transmitter Tests for DUT Type “Host” on 1-Port, 2-Lanes

4 Under the **Configure** tab, you may modify the values for various configurable options associated with the compliance tests. By default, the Thunderbolt Compliance Test Application sets the values of these options to the optimum value according to the standard specifications.

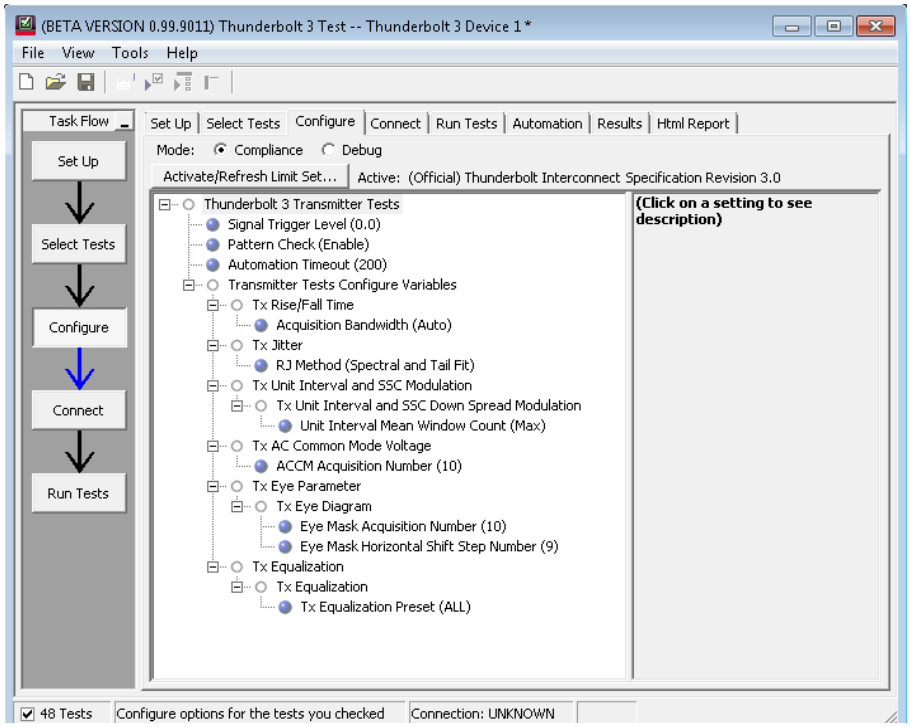


Figure 61 Configure options for Thunderbolt Tests

5 Under the **Connect** tab, the Thunderbolt Electrical Compliance Test Application displays a Connection Diagram along with a list of instructions. Figure 62 shows the connection diagram for a 2-Lane set up and Figure 63 shows the connection diagram for a 1-lane set up. If you have already set up a physical connection, you may verify else connect the DUT with the Oscilloscope as shown under this tab. Note that during some test runs, the application may prompt you for a change in physical connection/setup, as indicated in Figure 64.

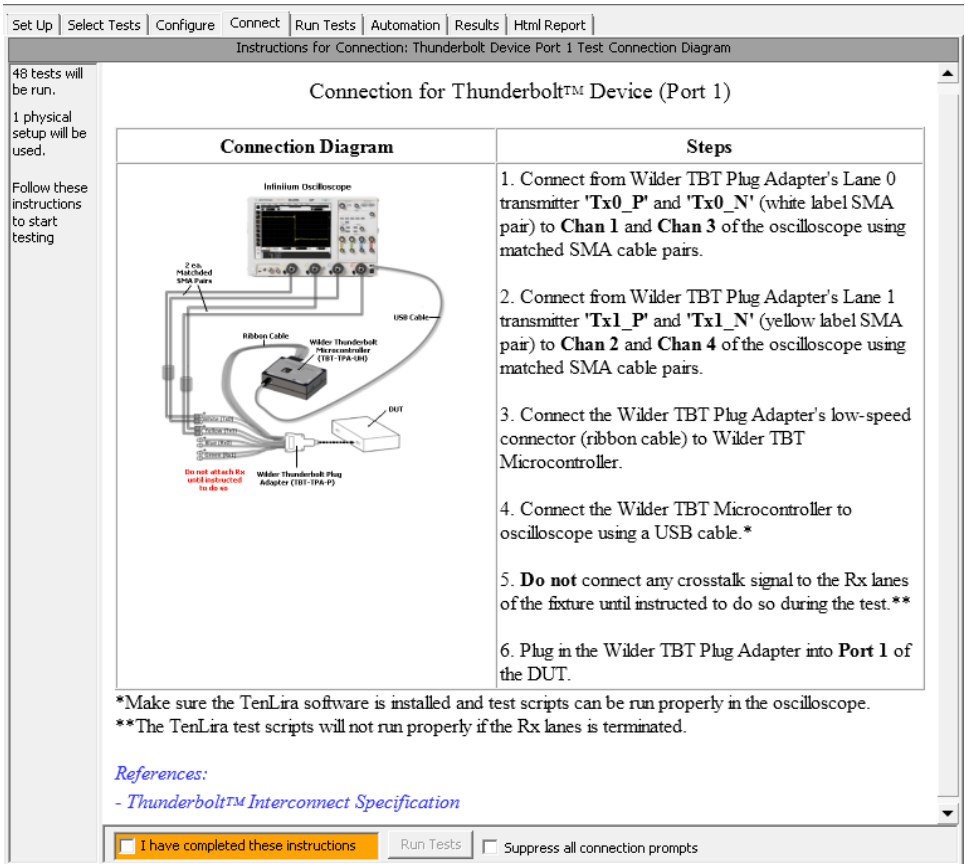


Figure 62 Connection Diagram and Instructions for a 2-Lane test set up

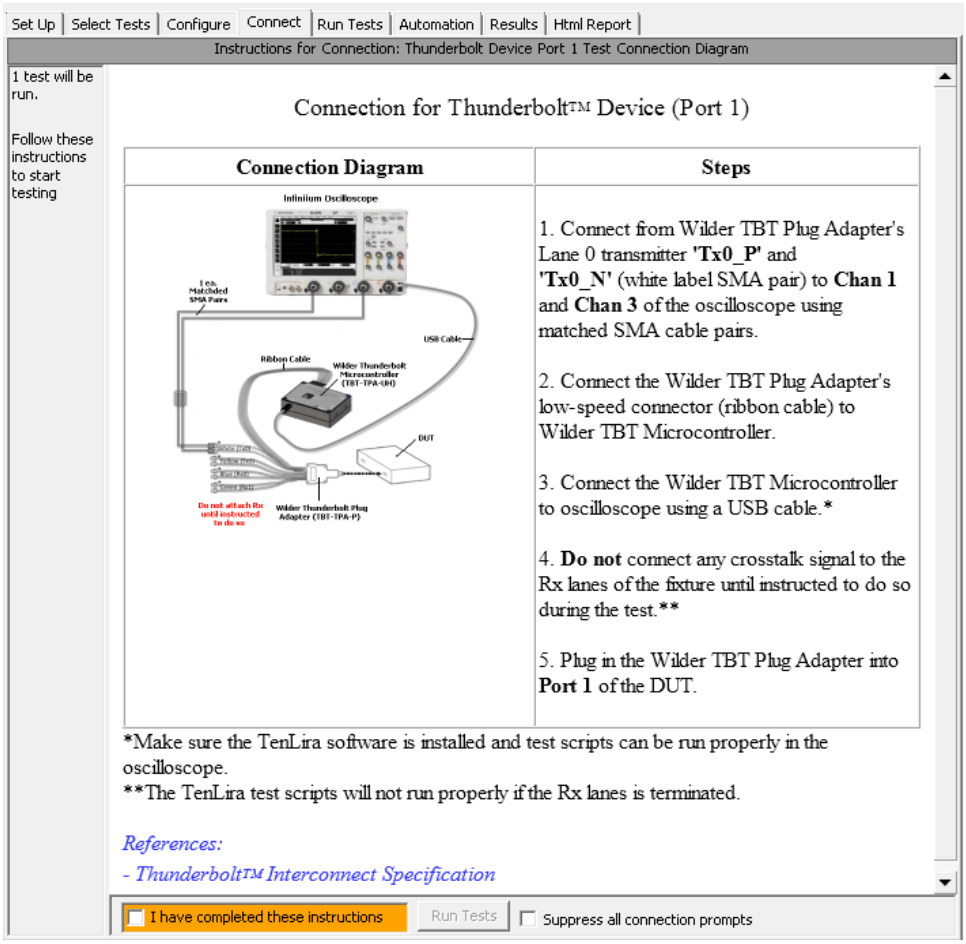


Figure 63 Connection Diagram and Instructions for a 1-Lane test set up

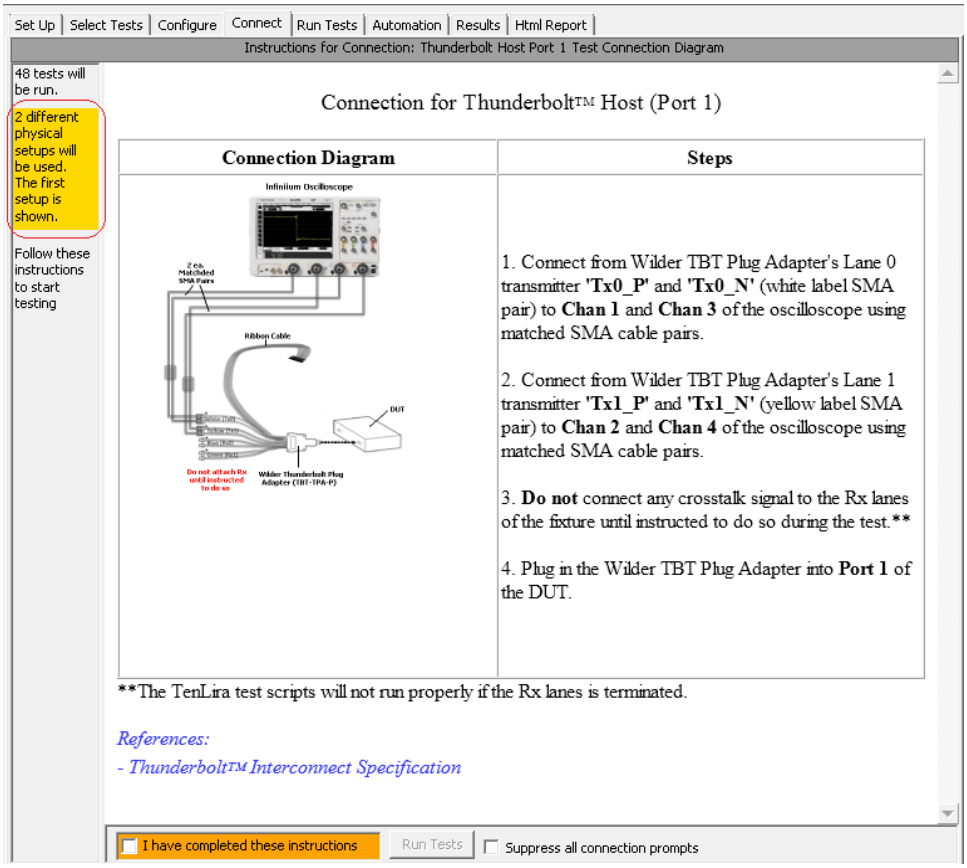


Figure 64 Indication for change of physical set up during test runs

6 Once you have performed steps 1 to 5, you are ready to run compliance tests on the Thunderbolt DUT. Additionally, you may configure/modify the run settings, automate options in the Test Application; view, export and print the test results and the HTML reports generated by the Test Application. Refer to the *Keysight N6470A Thunderbolt Electrical Compliance Test Application Online Help* to know more about how to use the Test Application.

Calibration Setup for Compliance Tests

Before running compliance tests on a Thunderbolt DUT, it is imperative that the testing equipment and its accessories be calibrated. The Thunderbolt Electrical Compliance Test Application provides the options to run Channel Skew Calibration and configure settings for Preset Calibration and CTLE Calibration.

Do the following:

1 Under the **Set Up** tab of the Thunderbolt Electrical Compliance Test Application, click the **Calibrate Setup** button.

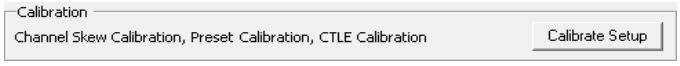


Figure 65 Calibration area under the **Set Up** tab

2 The **Calibration** window appears. It has three tabs—**Channel Skew Calibration**, **Preset Calibration** and **CTLE Calibration**. As shown in Figure 66, the **Channel Skew Calibration** tab view displays by default.

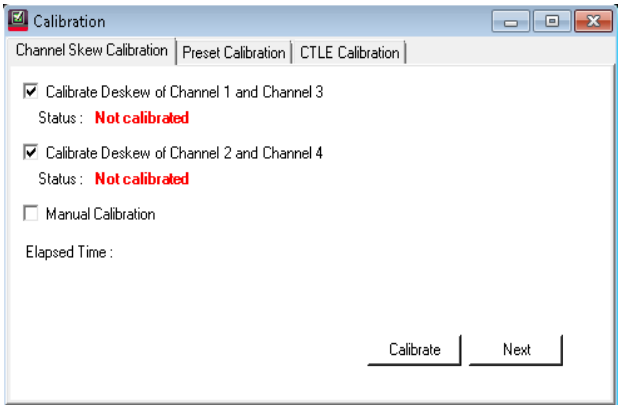


Figure 66 Default view of the **Calibration** window

Channel Skew Calibration

In order to achieve accurate test results and to verify that the Device under test is compliant to the standards, it is necessary to calibrate the Oscilloscope channels that are connected via cables to the Thunderbolt DUT.

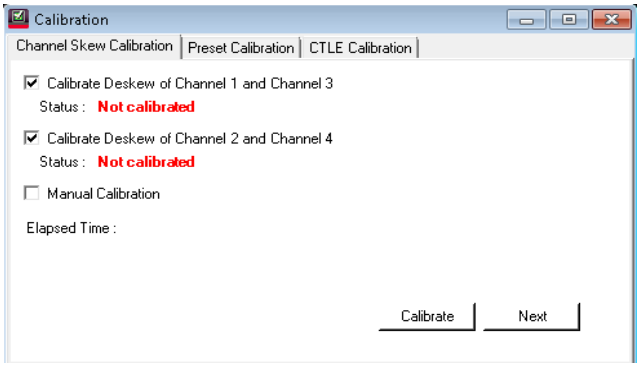


Figure 67 Channel Skew Calibration Options

Under the **Channel Skew Calibration** tab, the Thunderbolt Electrical Compliance Test Application displays the status of the Oscilloscope Channels that have been calibrated for de-skew. As shown in Figure 67, the options **Calibrate Deskew of Channel 1 and Channel 3** and **Calibrate Deskew of Channel 2 and Channel 4** are checked by default and the status of each of these options is **Not Calibrated**. You may also select the **Manual Calibration** check-box to perform Channel Skew Calibration later.

To start calibration of the selected Oscilloscope channel pairs, click the **Calibrate** button. The **Test Instruction for Thunderbolt 3 Compliance** window appears.

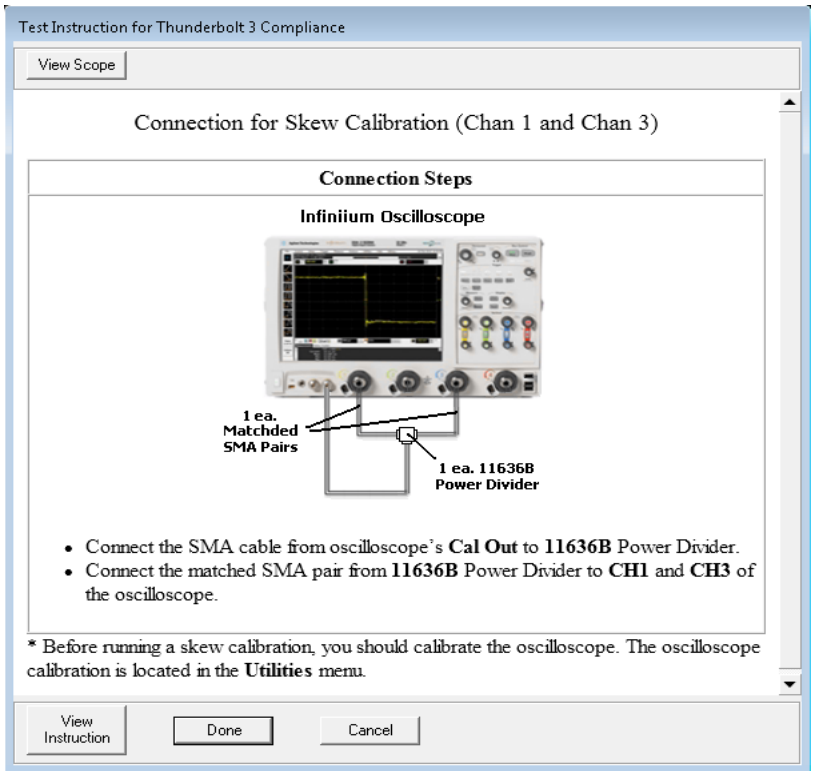


Figure 68 Instructions for Channel Skew Calibration for the selected Oscilloscope Channels

The **Test Instruction for Thunderbolt 3 Compliance** window provides instructions and connection diagram required to be set up to perform Channel Skew Calibration. Figure 68 shows the **Connection for Skew Calibration for Channel 1 and Channel 3**. Repeat these instructions for Skew Calibration for Channel 2 and Channel 4. Note that before you start performing Channel Skew Calibration, the Oscilloscope and probes must have been calibrated. If you have not already calibrated the oscilloscope and probe, see Chapter 6, "Calibrating the Infiniium Oscilloscope" to calibrate the Oscilloscope and probes.

On the **Test Instruction for Thunderbolt 3 Compliance** window,

1 Click the **View Scope** button to minimize this window and to see the Oscilloscope screen for the waveform and to use the Infiniium controls to perform Oscilloscope Calibration (if it has not been done yet).

2 Click the **View Instruction** button to maximize the window to view the instructions and the connection diagram again.

3 Once you have set up the physical connection for Channel Skew Calibration for the respective channels, click **Done** to begin Calibration. You may click **Cancel** at any point to simply return to the **Calibration** window.

4 When you click **Done**, the **Calibration** window displays again with the updated Status along with the time elapsed during this process, as shown in Figure 69:

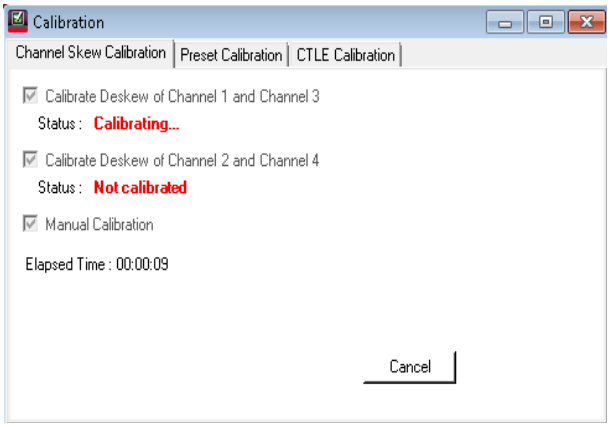


Figure 69 Calibration Status changes

Once the Calibration process is successfully done, the status changes to **Calibrated**. You may click **Cancel** to stop the process of Channel Skew Calibration at any time.

5 Before you begin Channel Skew Calibration or after the Channel Skew Calibration is complete, click the **Next** button to move to the next tab or click the tab, which you want to view.

Preset Calibration

The **Preset Calibration** tab allows you set the preset numbers on the Thunderbolt Electrical Compliance Test Application, which has been set on the Thunderbolt DUT, such that you can find the optimum preset.

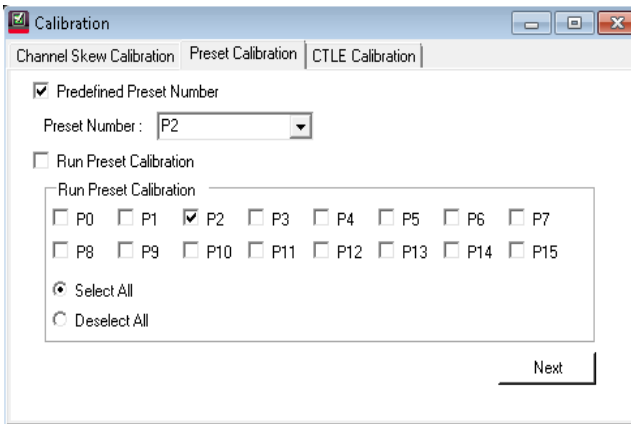


Figure 70 Default view of the Preset Calibration tab

Under the **Preset Calibration** tab,

1 By default, the **Predefined Preset Number** check-box is selected and the default Preset Number is set to **P2**.

2 From the **Preset Number :** drop-down, you may select another preset number that has been configured on the DUT.

3 Select the **Run Preset Calibration** check-box only if you wish to run Preset Calibration to find the optimum preset value for the DUT.

4 In the **Run Preset Calibration**, only **P2** is selected by default. You may select any of the preset numbers to include them for running preset calibration. You may use the **Select All** or **Deselect All** radio buttons to perform this action as well.

5 Click **Next** to move to the next tab or click the tab, which you want to view.

CTLE Calibration

The **CTLE Calibration** tab allows you set the Continuous-Time-Linear-Equalizer (CTLE) on the Thunderbolt Electrical Compliance Test Application, which has been set at the test point TP3EQ on the Thunderbolt DUT, such that you can find the optimum DC Gain value for the TP3EQ compliance tests.

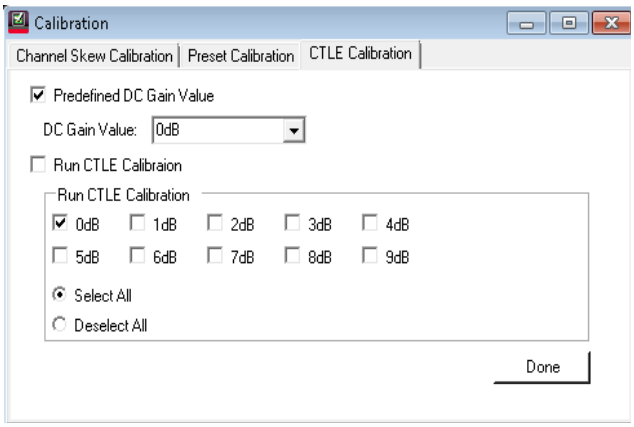


Figure 71 Default view of the CTLE Calibration tab

Under the **CTLE Calibration** tab,

1 By default, the **Predefined DC Gain Value** check-box is selected and the default DC Gain value is set to **0dB**.

2 From the **DC Gain Value:** drop-down, you may select another value for DC Gain that has been configured on the DUT.

3 Select the **Run CTLE Calibration** check-box only if you wish to run CTLE Calibration to find the optimum DC Gain value for the DUT.

4 In the **Run CTLE Calibration**, only **0dB** is selected by default. You may select any of the DC Gain values to include them for running CTLE calibration. You may use the **Select All** or **Deselect All** radio buttons to perform this action as well.

5 Click **Done** to save any modifications done to the **Calibration** window and to return to the Thunderbolt Test Environment Setup.

Tx Preset Calibration

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE **Prior to running the compliance tests, the Host / Device must go through Preset Calibration.**

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Preset Calibration* are checked.

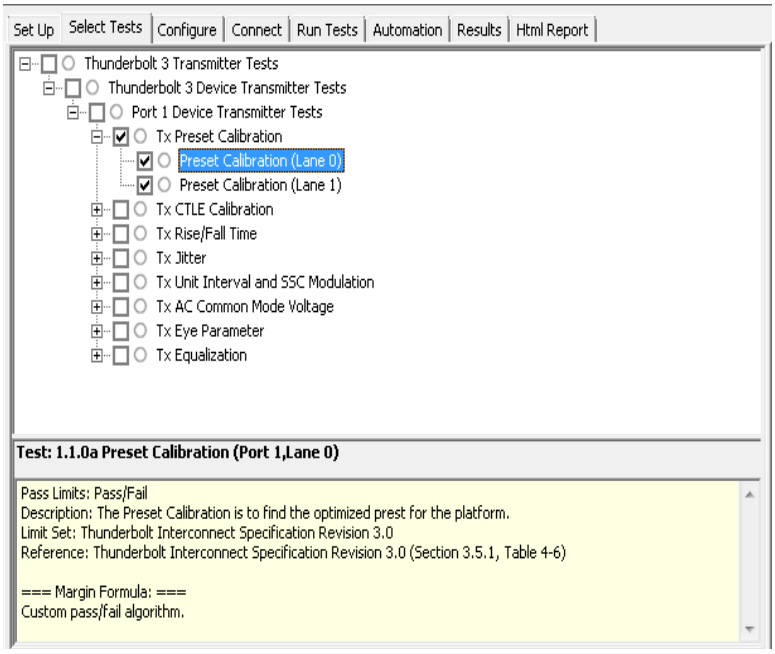


Figure 72 Selecting the Tx Preset Calibration tests

Test Procedure

1 Connect the DUT to the Oscilloscope.

2 Configure the DUT transmitter to output PRBS31, 20.625GB/s, Preset 0 (P0) on all lanes with SSC enabled.

3 Perform measurements with:
   a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.71; no average and no interpolation to be used; set to real time eye.
   b Oscilloscope with a bandwidth of 21±1GHz.
4 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate ≥ 50 GSa/s
   b Adjust vertical scale such that the signal fits on the Oscilloscope screen
   c Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
5 Capture eye height and eye width for lane 0.
6 Register eye height and eye width values.
7 Repeat the test for the remaining Thunderbolt lanes.
8 Repeat the test for all remaining Thunderbolt transmit presets (till preset 15 as shown in Table 5).
9 For each lane, choose the preset that provides maximum eye width. If there are two presets with the same eye width, choose the one with the greater eye height.

Expected / Observable Results

For each lane, the preset that provides the maximum eye width is the optimized preset for the platform. If two presets have the same eye width, the preset with a greater eye height is the optimized preset.

Test References

See

- "Section 3.3.2 Preset Calibration for 20.625 Gb/s" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-5 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx CTLE Calibration

Test Overview

The objective of the Tx CTLE Calibration Test is to find the optimized CTLE (Continuous-Time-Linear-Equalizer) for the platform.

See "Reference CTLE" on page 33 to know more about CTLE.

NOTE **Apply equalization on the Oscilloscope, when testing at TP3EQ.**

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx CTLE Calibration* are checked.

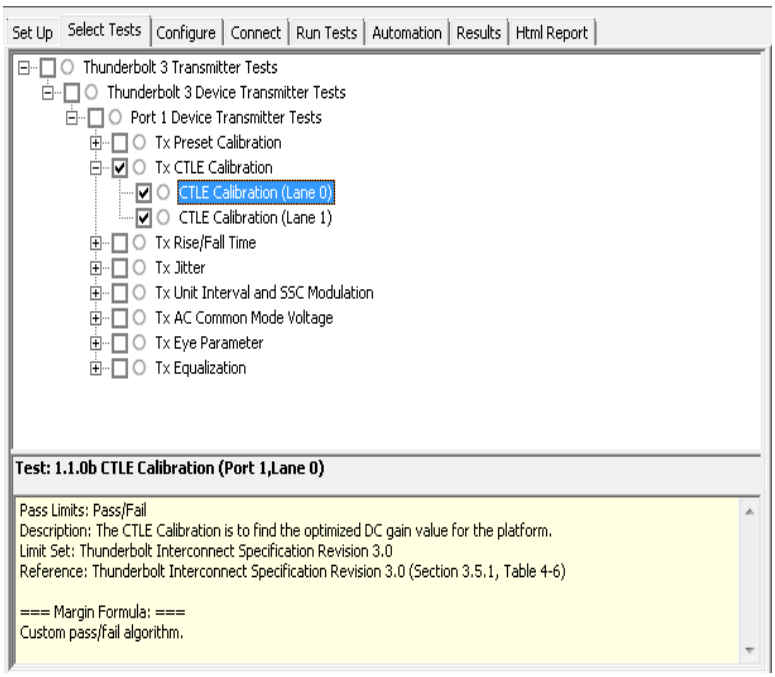


Figure 73 Selecting the Tx CTLE Calibration tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31, 20.625 GB/s with SSC enabled.
2. Perform measurements with:
   a. 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.71; no average and no interpolation to be used
   b. Oscilloscope with a bandwidth of 21±1GHz
   c. Set Oscilloscope to show real time eye
3. Follow the CTLE model as described in "Reference CTLE" on page 33, with the following parameters:
   a. AC Gain – 1.41
   b. Pole 1 – 5 G rad/sec
   c. Pole 2 – 10 G rad/sec
4. Calibrate DC Gain using the following equation:

$$\max_{\text{DC Gain}} (\text{eye height}),\ \text{DC Gain} = \{10^{-x/20} : x = 0 \div 9\ [\text{dB}]\}$$

5. Register eye height and eye width values.
6. Repeat the test for the remaining Thunderbolt lanes.
7. For each lane, choose the DC Gain value that provides maximum eye height. If there are two DC Gain values with the same eye height, choose the one with the greater eye width.
8. After optimizing the CTLE, apply automatic DFE (Decision-Feedback-Equalizer) with a maximum tap of 50mV. See "Reference DFE" on page 35 to know more about DFE.

Expected / Observable Results

For each lane, the DC Gain value that provides the maximum eye height is the optimized CTLE for the platform. If two DC Gain values have the same eye height, the one with a greater eye width is the optimized CTLE.

Test References

See

- "Section 5. Appendix A – CTLE Calibration" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Section 5.4.4.1 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Rise/Fall Time

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the Thunderbolt differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time $\geq$ 10ps (Refer to Table 4 on page 36).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.
2. Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.
3. Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Rise/Fall Time* are checked.

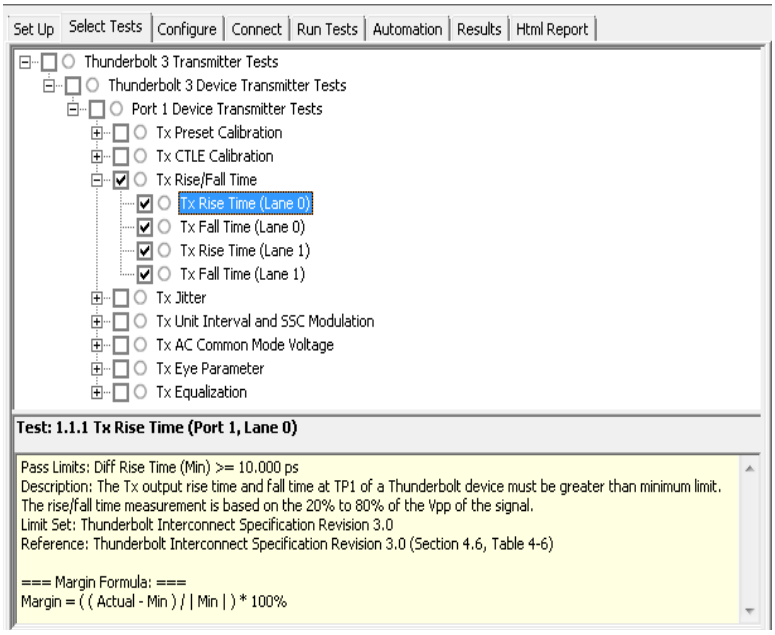


Figure 74 Selecting the Tx Rise/Fall Time tests

Test Procedure

1. Configure the DUT transmitter to output alternating square pattern of 32 0's and 32 1's on all lanes with SSC enabled.
2. Evaluate at least 4Mpts per channel (use the maximum analog bandwidth of the Oscilloscope). No CDR, no average and no interpolation to be used.
3. Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.

4 Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If T_{RISE} < 10ps, the status of test is FAIL.

If T_{FALL} < 10ps, the status of test is FAIL.

Test References

See

- "Section 3.5.8 Rise/Fall Time Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Total Jitter

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of 1 x 10^{-13}.

Test Pass Requirement

Total Jitter (TJ) $\leq$ 0.5 UI_{p-p} (Refer to Table 8 on page 43).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see “Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

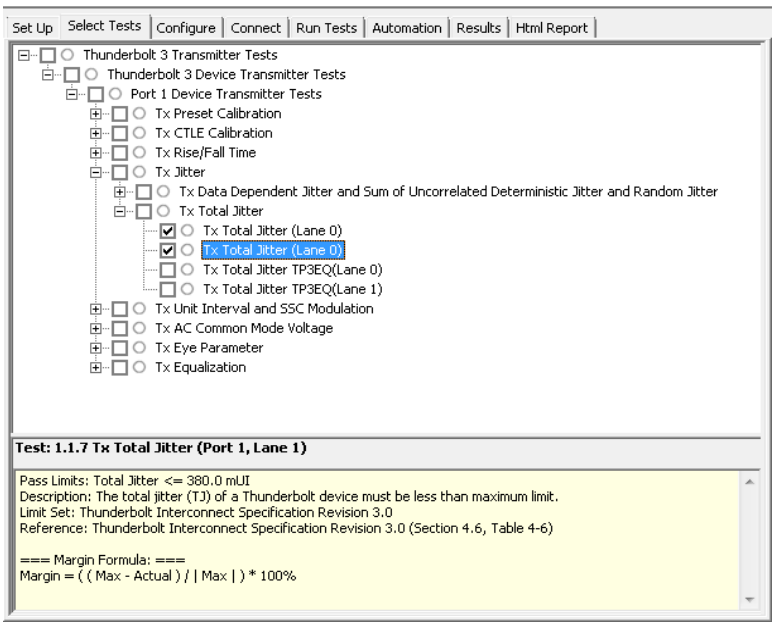


Figure 75 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Perform measurements with:

a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.71; no average and no interpolation to be used

b Oscilloscope with a bandwidth of 21±1GHz

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate ≥ 50 GSa/s
   b Pattern length – Arbitrary (at least -2, 11)
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
4 If TJ > 0.5 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
   b Perform measurements with:
   - 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.71; no average and no interpolation to be used
   - Oscilloscope with a bandwidth of 21±1GHz

   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate ≥ 50 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Adjust vertical scale such that the signal fits on the Oscilloscope screen
   - Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   - Referenced to 1E-13 statistics
   - Capture the Deterministic Jitter (DJ) result

   d Configure the DUT transmitter to output alternating square pattern of 1 0's and 1 1's (square pattern) on all lanes with SSC enabled.
   e Perform measurements with:
   - 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.71; no average and no interpolation to be used
   - Oscilloscope with a bandwidth of 21±1GHz

   f Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate ≥ 50 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Adjust vertical scale such that the signal fits on the Oscilloscope screen
   - Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   - Referenced to 1E-13 statistics
   - Capture the Random Jitter (RJ) result

   g Calculate TJ using the equation:

$$TJ = DJ + 14.7 * RJ$$

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If TJ > 0.5 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.9 Total Jitter" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Sum of Uncorrelated Jitter

Test Overview

The objective of the Tx Sum of Uncorrelated Jitter Test is to confirm that the sum of Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Sum of Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 8 on page 43).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Data Dependent Jitter and Sum of Uncorrelated Deterministic Jitter and Random Jitter* are checked.

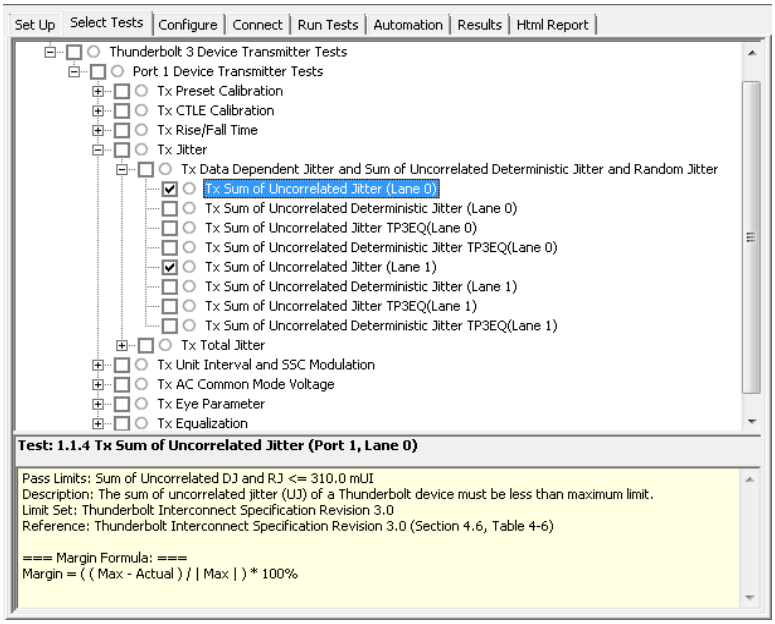


Figure 76 Selecting the Tx Sum of Uncorrelated Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.

2 Perform measurements with:

a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.71; no average and no interpolation to be used

b Oscilloscope with a bandwidth of 21±1GHz

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 50 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits on the Oscilloscope screen
   e Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   f Referenced to 1E-13 statistics
4 Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5 Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.10 UJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Sum of Uncorrelated Deterministic Jitter

Test Overview

The objective of the Tx Sum of Uncorrelated Deterministic Jitter Test is to confirm that the sum of Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Sum of Uncorrelated Deterministic Jitter (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 8 on page 43).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Data Dependent Jitter and Sum of Uncorrelated Deterministic Jitter and Random Jitter* are checked.

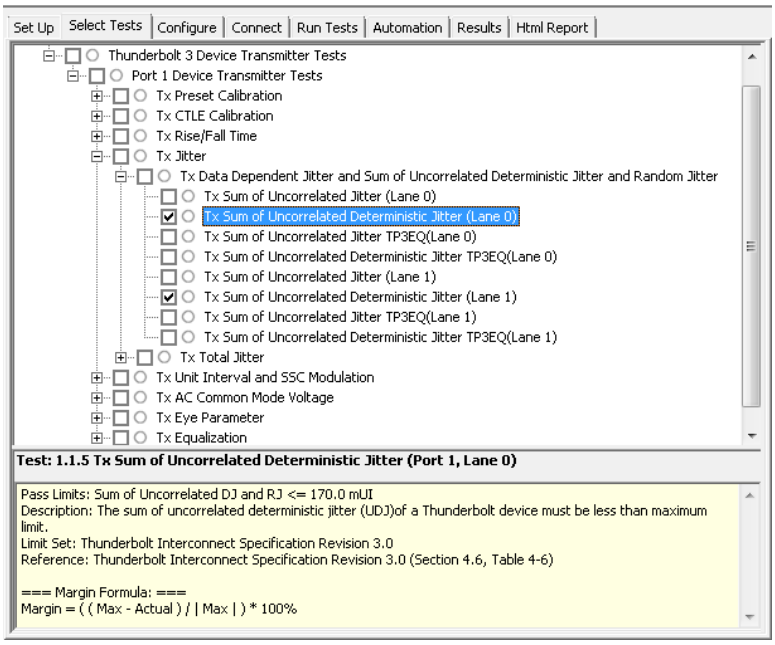


Figure 77 Selecting the Tx Sum of Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.

2 Perform measurements with:

a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.71; no average and no interpolation to be used

b Oscilloscope with a bandwidth of 21±1GHz

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 50 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits on the Oscilloscope screen
   e Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   f Referenced to 1E-13 statistics
4 Capture the BUJ result.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.11 UDJ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Unit Interval

Test Overview

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

48.4703ps ≤ Unit Interval ≤ 48.7432ps (Refer to Table 8 on page 43).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

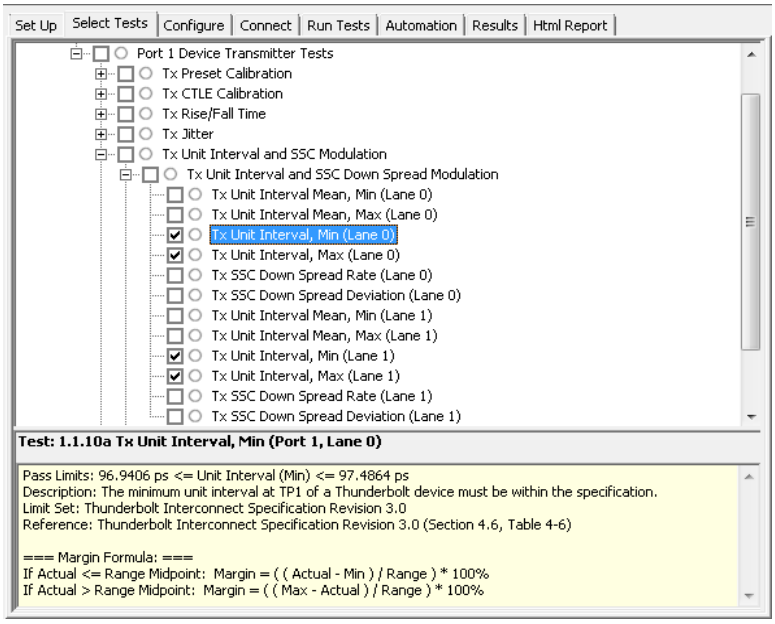


Figure 78 Selecting the Tx Unit Interval tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 26Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 21±1GHz

3 Calculate UI dynamically using the moving average procedure with a window size of 3000 symbols. Measure the values of both UI_{MAX} and UI_{MIN}.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If UI_{MAX} > 48.4703ps, the status of test is FAIL.

If UI_{MIN} < 48.7432ps, the status of test is FAIL.

Test References

See

- "Section 3.5.2 Unit Interval Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Unit Interval Mean

Test Overview

The objective of the Tx Unit Interval Mean Test is to confirm that the average data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

48.5917ps ≤ Average Unit Interval ≤ 48.6210ps (Refer to Table 8 on page 43).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

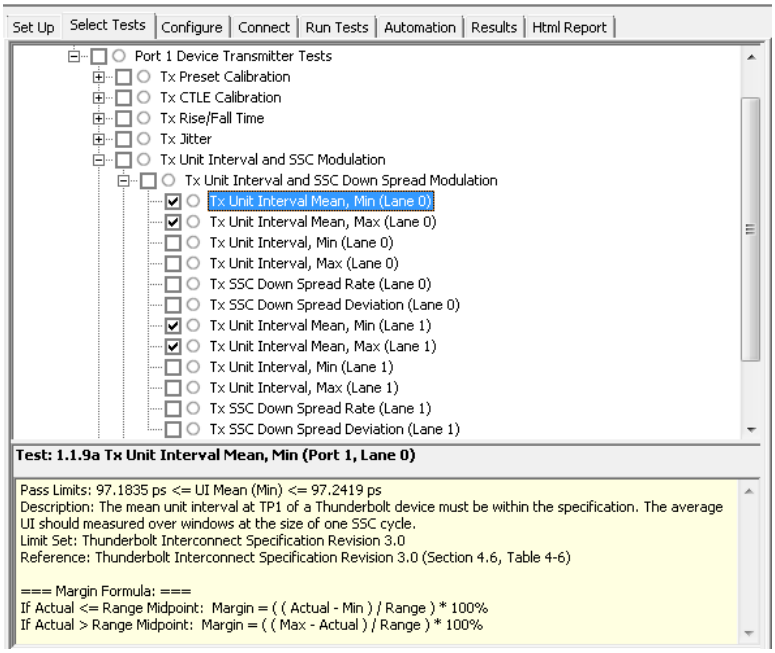


Figure 79 Selecting the Tx Unit Interval Mean tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 26Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 21±1GHz

3 Use mathematical analysis to measure the average unit interval over window at the size of one SSC cycle, determined by the SSC_Down_Spread_Rate.

4 Measure UI_MEAN over different windows that uniformly cover the scope capture over at least 300ms (more than 10 SSC Cycles) with 10000 UI window jumps. See Figure 80.

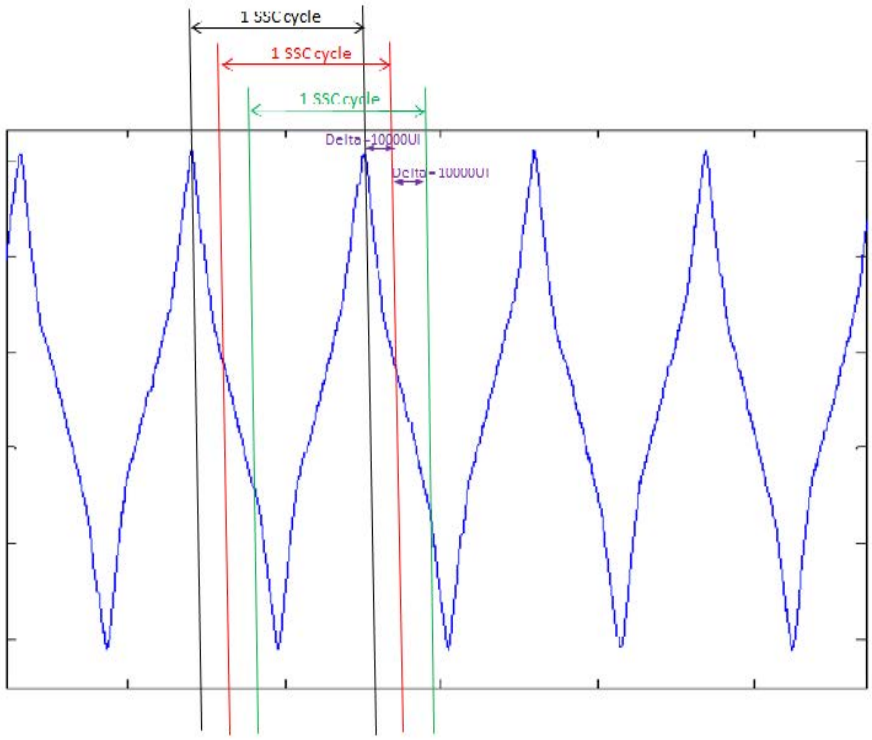


Figure 80 Measurement of UI_MEAN over at least 10 SSC Cycles

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the maximum UI_MEAN measured > 48.6210ps, the status of test is FAIL.

If the minimum UI_MEAN measured < 48.5917ps, the status of test is FAIL.

Test References

See

- "Section 3.5.3 Unit Interval Mean Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx SSC Down Spread Deviation

Test Overview

The objective of the Tx SSC Down Spread Deviation Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

-0.03% ≤ SSC_Down_Spread_Deviation ≤ 0.53% (Refer to Table 4 on page 36).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.
2. Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.
3. Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

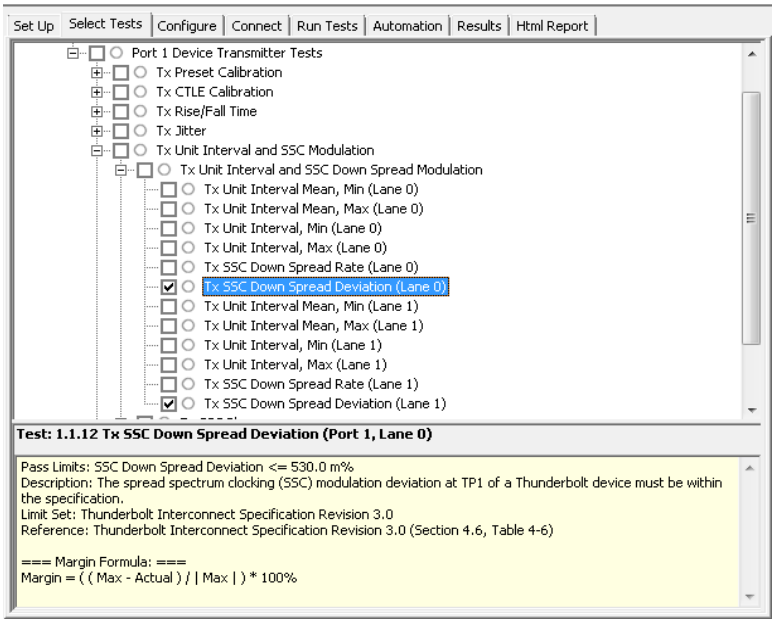


Figure 81 Selecting the Tx SSC Down Spread Deviation tests

Test Procedure

1. Run the "Tx Unit Interval" Test as a prerequisite to obtain UI_{MAX}.
2. Use the obtained value of UI_{MAX} to calculate the Deviation percentage:

$$Deviation = 100*\{[(1 / UI_{MAX}) - 20.625GB/s] / 20.625GB/s\}$$

Expected / Observable Results

If SSC_Down_Spread_Deviation > 0.53% or SSC_Down_Spread_Deviation < -0.03%, the status of test is FAIL.

Test References

See

- “Section 3.5.4 SSC Down Spread Deviation Measurements” of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5.*

Tx SSC Down Spread Rate

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

35KHz ≤ SSC_Down_Spread_Rate ≤ 37KHz (Refer to Table 4 on page 36).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

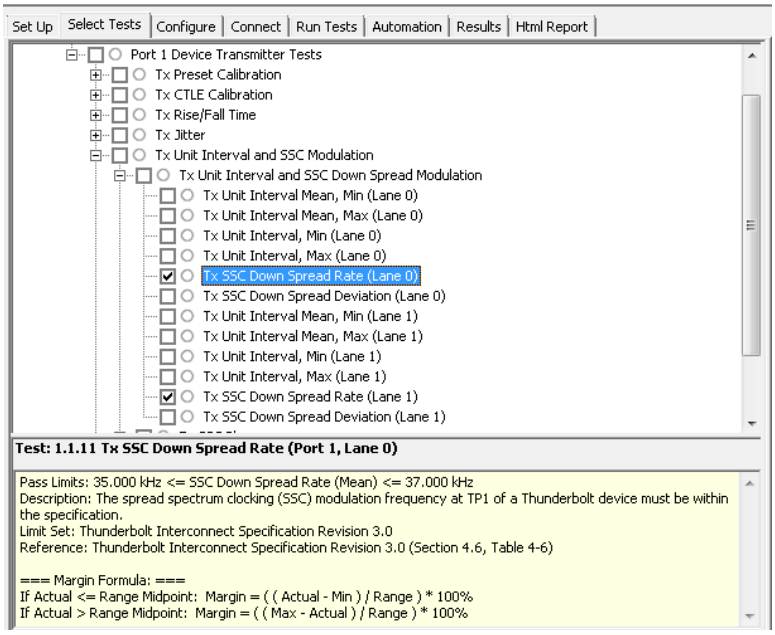


Figure 82 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 26Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 21±1GHz

3 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If 35KHz > SSC_Down_Spread_Rate > 37KHz, the status of test is FAIL.

Test References

See

- "Section 3.5.5 SSC Down Spread Rate Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5.*

Tx SSC Phase Deviation

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.5ns p-p ≤ SSC_Phase_Deviation ≤ 16.5ns p-p (Refer to Table 4 on page 36).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx SSC Phase* are checked.

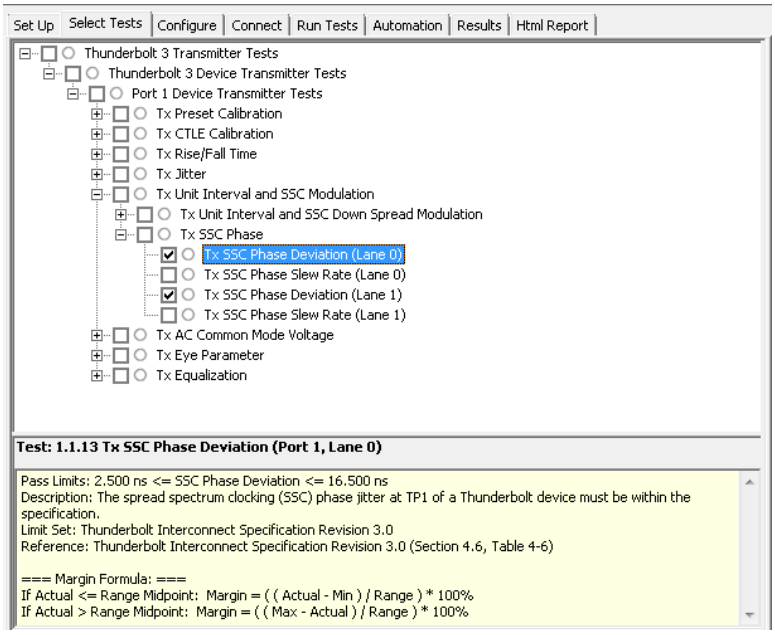


Figure 83 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and post process it with an appropriate software:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 40Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 21±1GHz

3 Extract the SSC Phase Deviation from the transmitted signal. The SSC Phase Deviation should be extracted from the phase jitter after applying a 2nd order low-pass filter with 3dB point at 5 MHz, damping factor 0.71.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If 2.5ns p-p > SSC_Phase_Deviation > 16.5ns p-p, the status of test is FAIL.

Test References

See

- "Section 3.5.6 SSC Phase Deviation Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx SSC Phase Slew Rate

Test Overview

The objective of the Tx SSC Phase Slew Rate Test is to confirm that the SSC Phase Jitter Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Phase_Slew_Rate ≤ 3.3ms/s (Refer to Table 4 on page 36).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx SSC Phase* are checked.

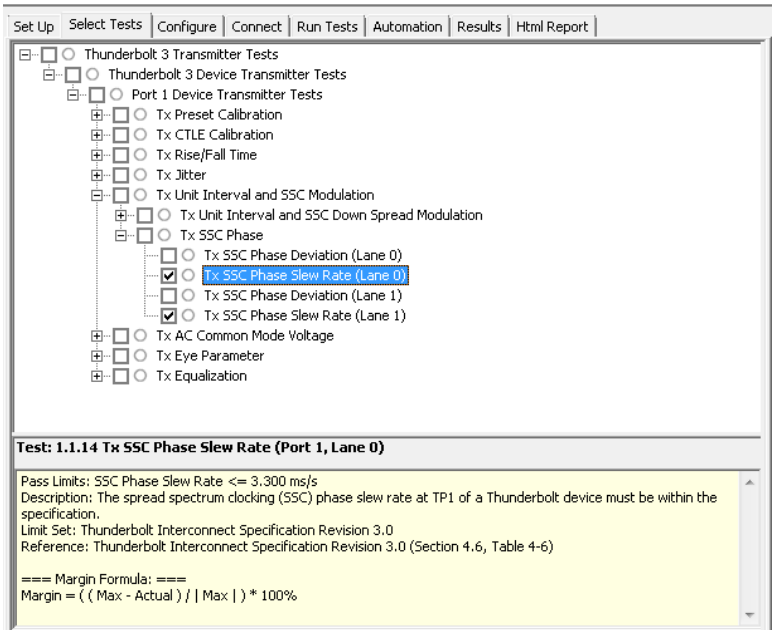


Figure 84 Selecting the Tx SSC Phase Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and post process it with an appropriate software:

a Sampling Rate ≥ 50 GSa/s

b Evaluate 40Mpts per channel and horizontal scale of 25 µs / square

c No CDR, no average and no interpolation to be used

d Oscilloscope must have a bandwidth of 21±1GHz

3 Extract the SSC Phase Slew Rate from the transmitted signal. The SSC Slew Rate should be extracted from the phase jitter after applying a 2nd order low-pass filter with 3dB point at 5 MHz, damping factor 0.71.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If SSC_Phase_Slew_Rate > 3.3ms/s, the status of test is FAIL.

Test References

See

- "Section 3.5.7 SSC Phase Slew Rate Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-4 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Eye Diagram

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 85.

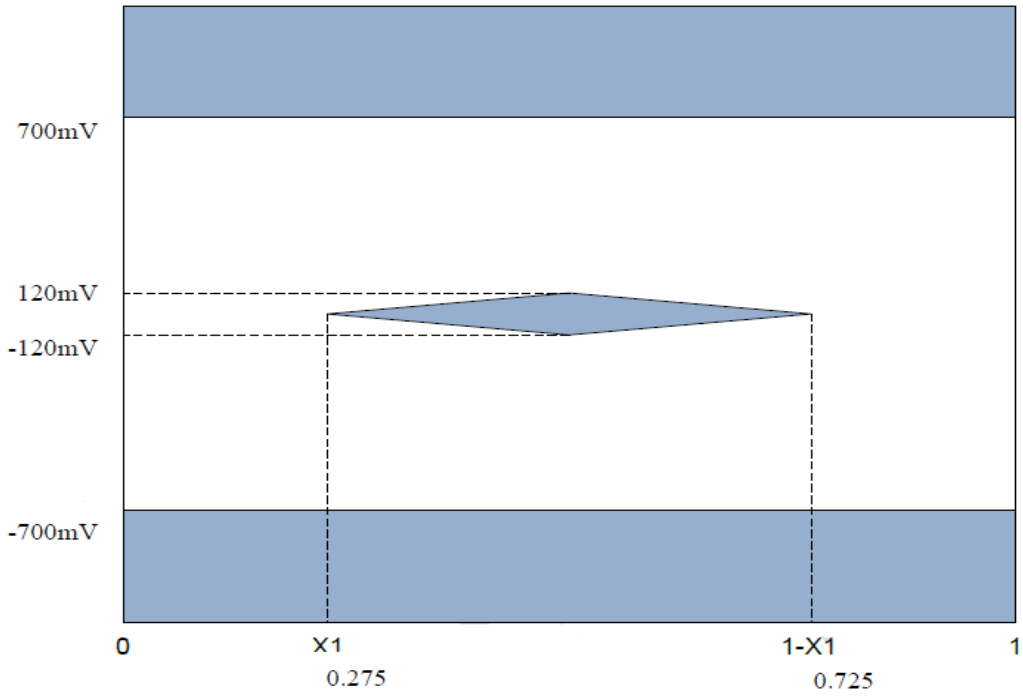


Figure 85 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 8 on page 43 and Figure 17 on page 42).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see “Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

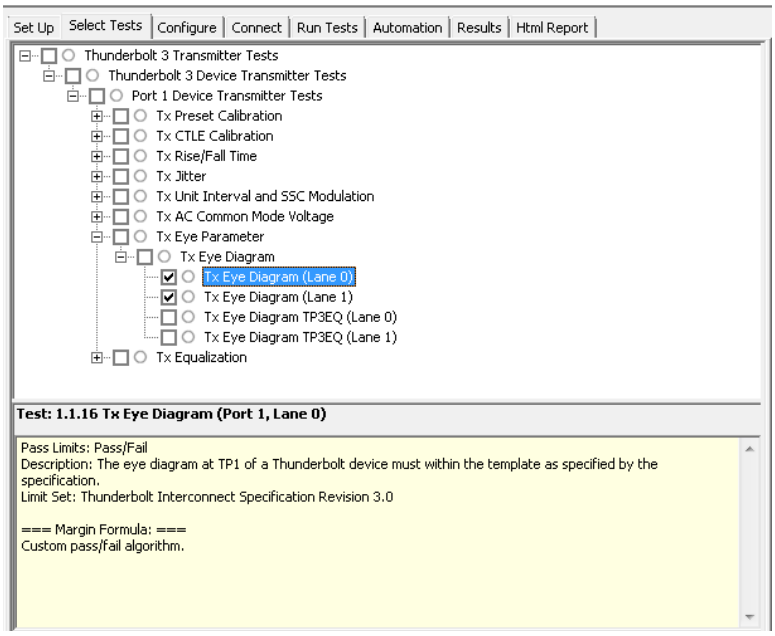


Figure 86 Selecting the Tx Eye Diagram tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate $\geq$ 50 GSa/s

b Perform measurements with a 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5MHz and damping factor of 0.71. No average and no interpolation to be used. Oscilloscope must have a bandwidth of 21±1GHz

c Accumulate at least 1E6 bits, adjust the memory depth and test duration in order to obtain at least 10 waveforms

3 Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section “Expected / Observable Results”.

4 Measure and save the inner eye height peak voltage of the signal for AC Common Mode Test (peak inner eye).

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/- 700mV), the status of the test is FAIL.

ii Shift the mask left or right through one entire T_{BIT} to determine if any horizontal position has no capture points within the eye mask. No vertical shifting of the mask is allowed.

iii If no such shifted position exists where no part of the waveform touches or crosses into the data eye, the status of the test is FAIL.

Test References

See

- "Section 3.5.12 Eye Diagram Measurement" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-8 and Figure 5-11 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx AC Common Mode Voltage

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the Thunderbolt differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq 80mV_{p-p}$ for systems with peak inner eye < 100mV (Low Swing).

TX AC Common Mode Voltage $\leq 100mV_{p-p}$ for systems with peak inner eye > 100mV (High Swing).

(Refer to Table 8 on page 43).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx AC Common Mode Voltage* are checked.

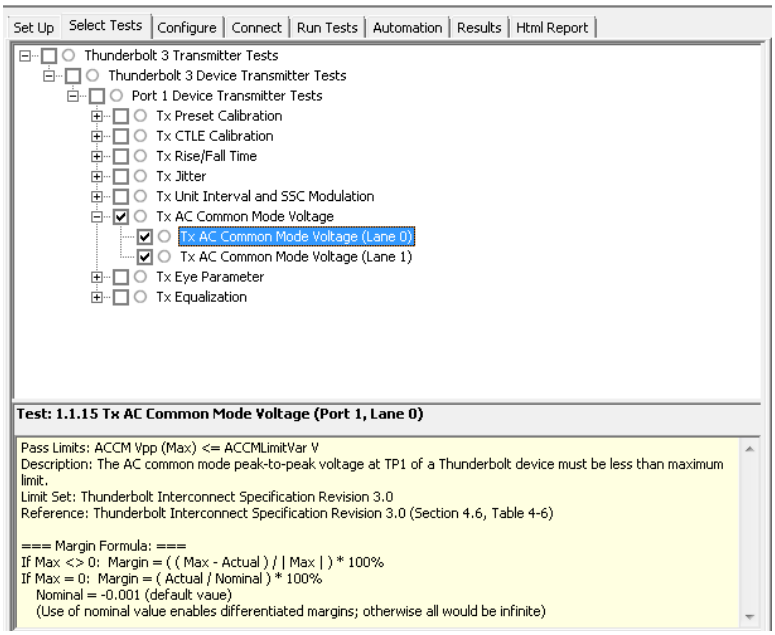


Figure 87 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 50 GSa/s
   b Evaluate 26Mpts per channel
   c Set vertical scale to 20mV/Div
   d No CDR, no average and no interpolation to be used
   e Oscilloscope must have a bandwidth of 21±1GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $V_{AC-CM} > 80mV_{p-p}$, the status of test is FAIL, for Low Swing.

If $V_{AC-CM} > 100mV_{p-p}$, the status of test is FAIL, for High Swing.

Test References

See

- "Section 3.5.13 AC Common Mode Measurements" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-8 of the *Thunderbolt Interconnect Specification Rev 1.5.*

Tx Equalization Tests

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Pre-shoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Pre-shoot, De-Emphasis: ± 1dB for the following presets:

Table 11 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.7
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	4.3	-9.3
15	1.7	-1.7

(Refer to Table 5 on page 38).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see “Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Equalization* are checked.

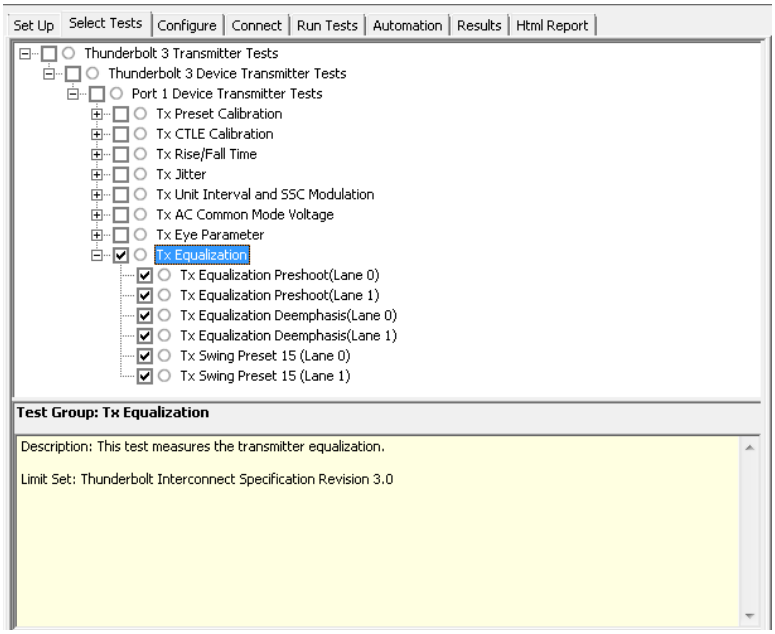


Figure 88 Selecting the Tx Equalization tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the Configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

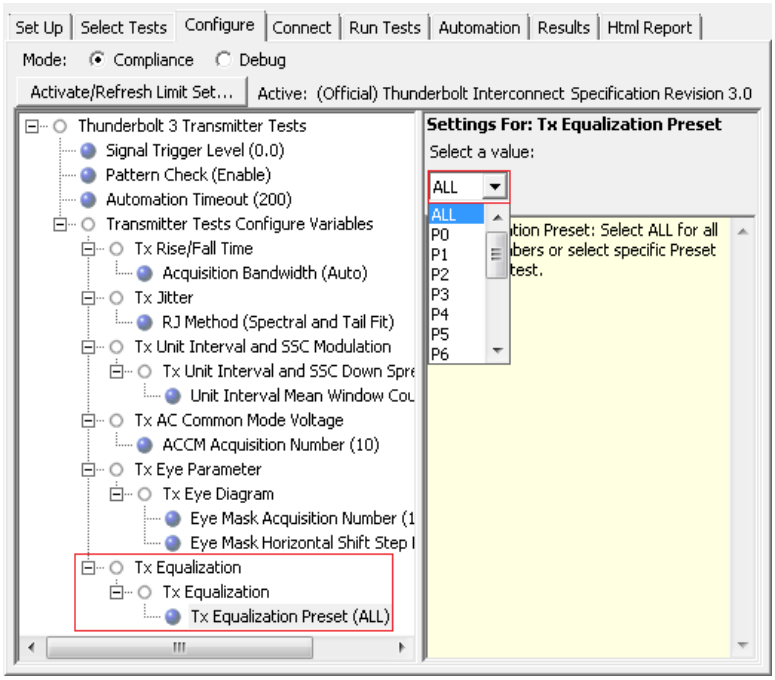


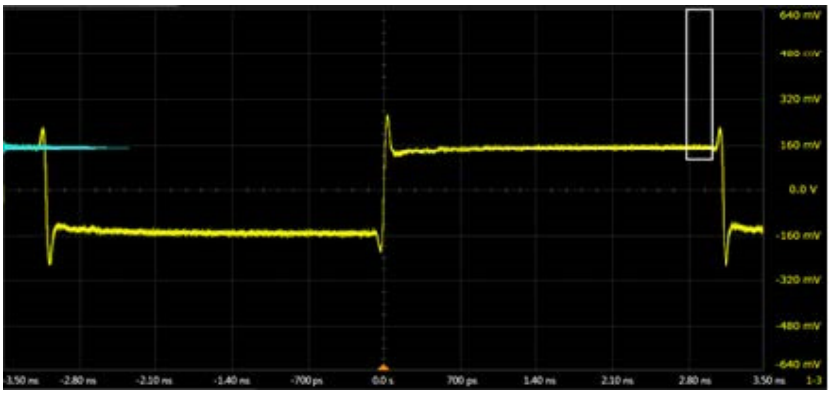
Figure 89 Configuring Tx Equalization Preset Variable

Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 21±1GHz.

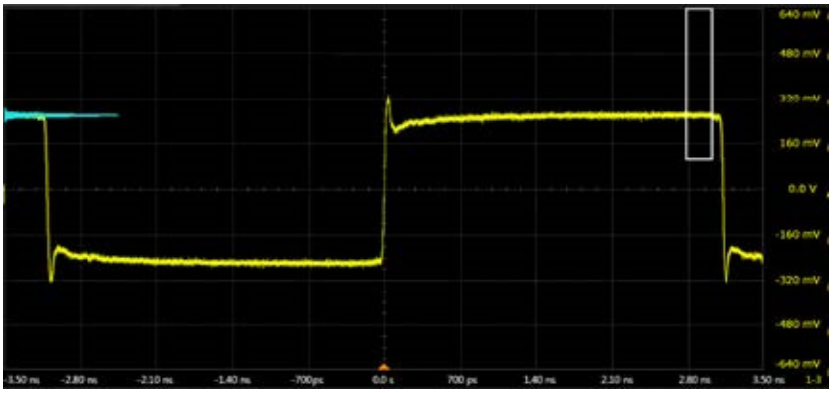


4 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

5 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

6 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 21±1GHz.

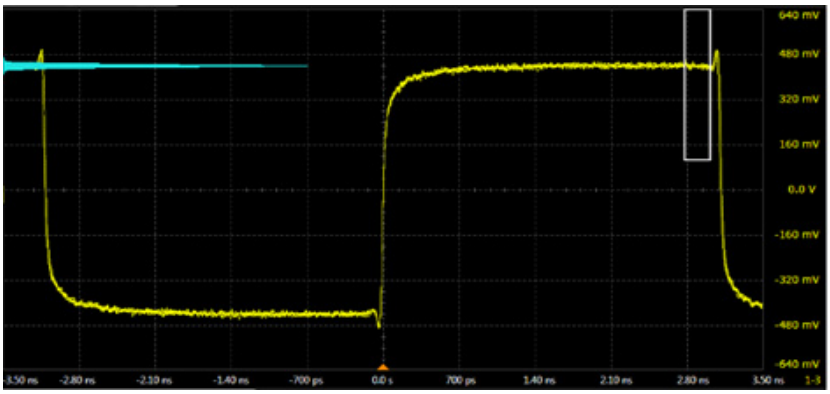


7 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

8 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

9 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 21±1GHz.



10 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

Set Pre-Shoot to be $20 * \log_{10} [V_2/V_1]$

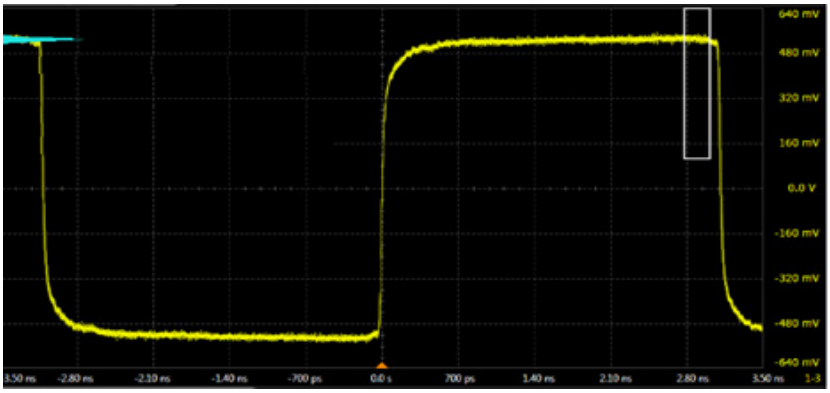
Set De-Emphasis to be $20 * \log_{10} [V_1/V_3]$

11 Repeat steps 2 to 10 for all Presets defined in Table 11.

12 Set the DUT to Preset 0 (P0).

13 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

14 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 21±1GHz.



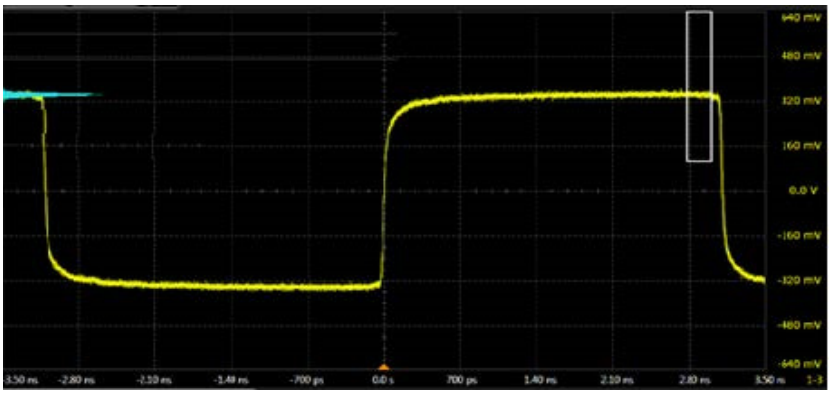
15 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

$$V_0 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

16 Set the DUT to Preset 15 (P15).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a bandwidth of 21±1GHz.



19 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Swing to be } 20 * \log_{10} [V_0/V_{15}]$$

20 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 11, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 11, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- "Section 3.5.1 Transmitter Equalization" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-5 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Total Jitter TP3EQ

Test Overview

The objective of the Tx Total Jitter TP3EQ Test is to confirm that the Total Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ_{TP3EQ}) ≤ 0.66 UI_{p-p} (Refer to Table 9 on page 44).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see “Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see “Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to “Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Total Jitter* are checked.

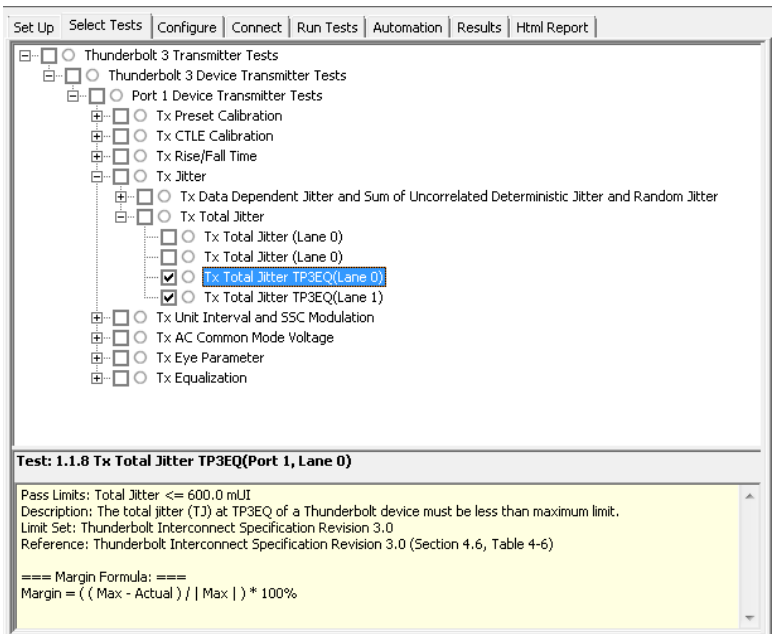


Figure 90 Selecting the Tx Total Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Ensure that measurements are done with a calibrated CTLE. See “Tx CTLE Calibration" on page 117.

3 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 50 GSa/s

b Pattern length – Arbitrary (at least -2, 11)

c Evaluate 26Mpts per channel and horizontal scale of 25 µs / square

4 If TJ > 0.66 UI_{p-p}, perform the following steps:

a Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.

b Ensure that measurements are done with a calibrated CTLE. See "Tx CTLE Calibration" on page 117.

c Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate ≥ 50 GSa/s
- Pattern length – Periodic
- Jitter Separation method must be suitable for cross-talk on the signal
- Adjust vertical scale such that the signal fits on the Oscilloscope screen
- Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
- Referenced to 1E-13 statistics
- Capture the Deterministic Jitter (DJ_{TP3EQ}) result

d Configure the DUT transmitter to output alternating square pattern of 1 0's and 1 1's (square pattern) on all lanes with SSC enabled.

e Perform measurements with:

- 2nd order CDR with closed loop rejection bandwidth (3 dB point) of 5 MHz and damping factor of 0.71; no average and no interpolation to be used

f Capture the waveform and process it with the Digital Oscilloscope:

- Sampling Rate ≥ 50 GSa/s
- Pattern length – Periodic
- Adjust vertical scale such that the signal fits on the Oscilloscope screen
- Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
- Referenced to 1E-13 statistics
- Capture the Random Jitter (RJ_{TP3EQ}) result

g Calculate TJ_{TP3EQ} using the equation:

$$TJ_{TP3EQ} = DJ_{TP3EQ} + 14.7 * RJ_{TP3EQ}$$

5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If TJ_{TP3EQ} > 0.66 UI_{p-p}, the status of test is FAIL.

Test References

See

- "Section 3.5.14 Total Jitter TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-9 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Sum of Uncorrelated Jitter TP3EQ

Test Overview

The objective of the Tx Sum of Uncorrelated Jitter TP3EQ Test is to confirm that the sum of Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Sum of Uncorrelated Jitter (UJ_{TP3EQ}) ≤ 0.33 UI_{p-p} (Refer to Table 9 on page 44).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Data Dependent Jitter and Sum of Uncorrelated Deterministic Jitter and Random Jitter* are checked.

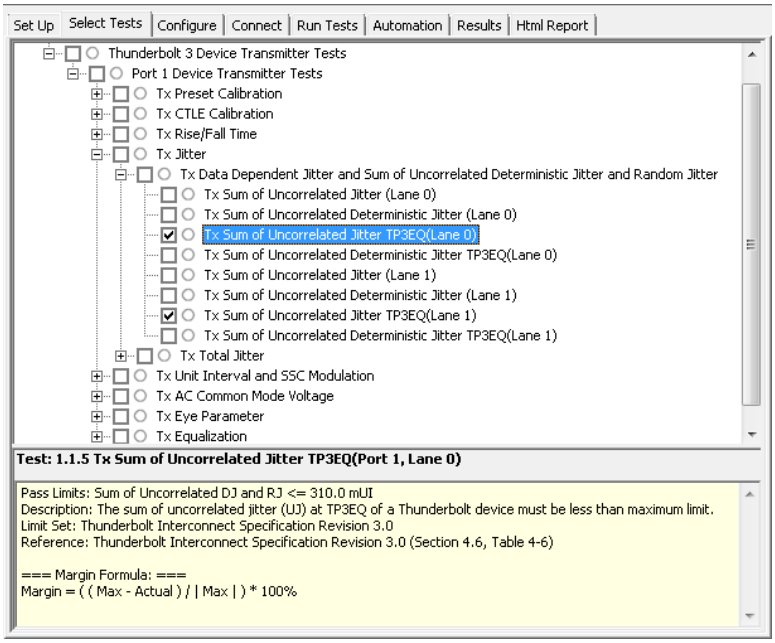


Figure 91 Selecting the Tx Sum of Uncorrelated Jitter TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.

2 Ensure that measurements are done with a calibrated CTLE. See "Tx CTLE Calibration" on page 117.

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 50 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits on the Oscilloscope screen
   e Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   f Referenced to 1E-13 statistics
4 Capture the Total Jitter (TJ_{TP3EQ}) and Data Dependent Jitter (DDJ_{TP3EQ}) results.
5 Calculate UJ_{TP3EQ} using the equation:

$$UJ_{TP3EQ} = TJ_{TP3EQ} - DDJ_{TP3EQ}$$

6 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UJ_{TP3EQ} > 0.33\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.15 UJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-9 of the *Thunderbolt Interconnect Specification Rev 1.5.*

Tx Sum of Uncorrelated Deterministic Jitter TP3EQ

Test Overview

The objective of the Tx Sum of Uncorrelated Deterministic Jitter TP3EQ Test is to confirm that the sum of Uncorrelated Deterministic Jitter at point TP3EQ of the transmitter is within the limits of the specification.

Test Pass Requirement

Sum of Uncorrelated Deterministic Jitter (UDJ_{TP3EQ}) ≤ 0.17 UI_{p-p} (Refer to Table 9 on page 44).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.
2. Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.
3. Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Data Dependent Jitter and Sum of Uncorrelated Deterministic Jitter and Random Jitter* are checked.

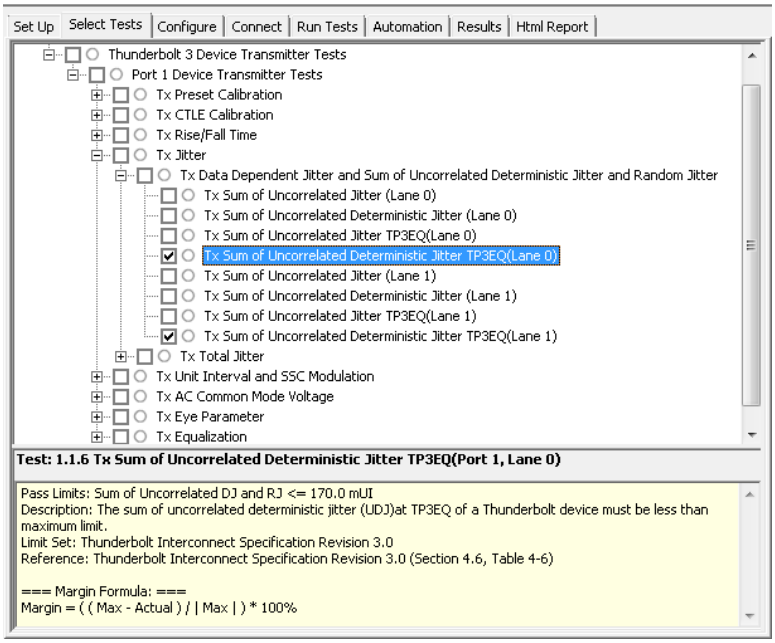


Figure 92 Selecting the Tx Sum of Uncorrelated Deterministic Jitter TP3EQ tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Ensure that measurements are done with a calibrated CTLE. See "Tx CTLE Calibration" on page 117.

3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate ≥ 50 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits on the Oscilloscope screen
   e Evaluate 26Mpts per channel and horizontal scale of 25 µs / square
   f Referenced to 1E-13 statistics
4 Capture the BUJ result.
5 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

If $UDJ_{TP3EQ} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- "Section 3.5.16 UDJ TP3EQ" of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-9 of the *Thunderbolt Interconnect Specification Rev 1.5*.

Tx Eye Diagram TP3EQ

Test Overview

The objective of the Tx Eye Diagram TP3EQ Test is to confirm that the differential signal on each Thunderbolt differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3EQ should meet the conditions depicted in Figure 93.

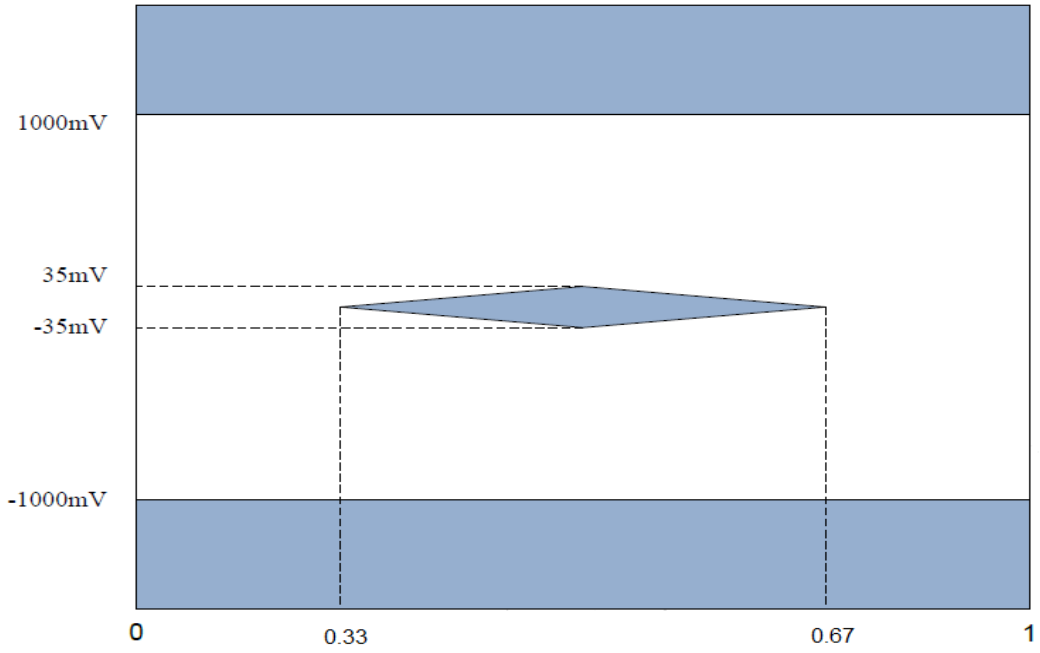


Figure 93 Pass Condition for Tx Eye Diagram TP3EQ Tests

(Refer to Table 9 on page 44 and Figure 17 on page 42).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter Test Setup" on page 45 and for configuring the Thunderbolt Electrical Compliance Test Application, see "Setting Up Test Application for 20.625 GB/s Systems" on page 104.

2 Perform Channel Skew Calibration is performed and configure settings for Preset Calibration and CTLE Calibration. Refer to "Calibration Setup for Compliance Tests" on page 111.

3 Under the **Select Tests** tab of the Thunderbolt Electrical Compliance Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

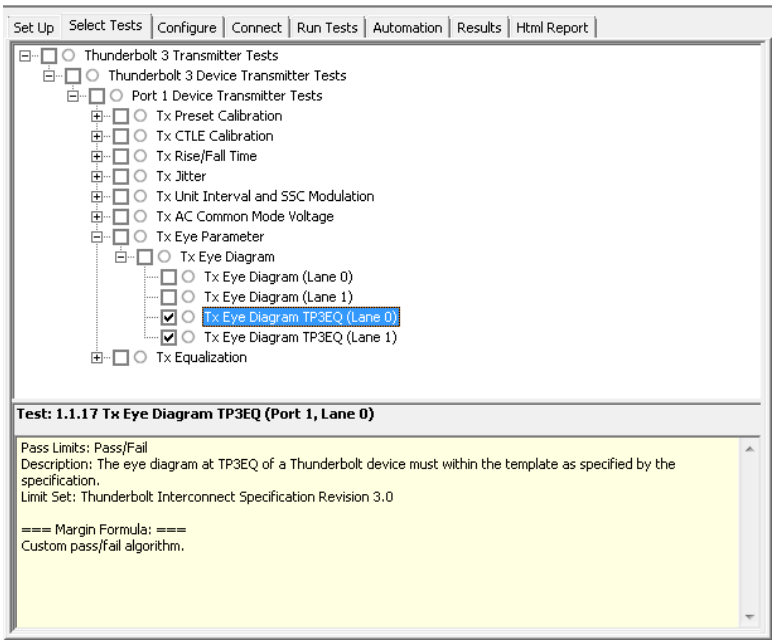


Figure 94 Selecting the Tx Eye Diagram TP3EQ tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate ≥ 50 GSa/s

b Ensure that measurements are done with a calibrated CTLE. See "Tx CTLE Calibration" on page 117.

c Accumulate at least 1E6 bits, adjust the memory depth and test duration in order to obtain at least 10 waveforms

3 Compare the data eye to the TP3EQ eye diagram mask. Check for conditions described in the section “Expected / Observable Results”.

4 Repeat the test for the remaining Thunderbolt lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/-1000mV), the status of the test is FAIL.

ii Shift the mask left or right through one entire T_{BIT} to determine if any horizontal position has no capture points within the eye mask. No vertical shifting of the mask is allowed.

iii If no such shifted position exists where no part of the waveform touches or crosses into the data eye, the status of the test is FAIL.

Test References

See

- “Section 3.5.17 Eye Diagram Measurement TP3EQ” of the *USB Type-C Thunderbolt Alternate Mode Electrical Host \ Device Compliance Test Specification Version 1.5*.
- Table 5-9 and Figure 5-11 of the *Thunderbolt Interconnect Specification Rev 1.5*.

6 Calibrating the Infiniium Oscilloscope

This section describes the Keysight Infiniium Oscilloscopes calibration procedures.

Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the Thunderbolt Electrical Compliance tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2 (provided with the Keysight Infiniium oscilloscope).
- Calibration cable (provided with the Keysight Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.

To Run the Self Calibration

NOTE **Let the Oscilloscope warm up before adjusting. Warm up the Oscilloscope for 30 minutes before starting calibration procedure. Failure to allow warm up may result in inaccurate calibration.**

The self calibration uses signals generated in the Oscilloscope to calibrate Channel sensitivity, offsets, and trigger parameters. You should run the self calibration

- yearly or according to your periodic needs,
- when you replace the acquisition assembly or acquisition hybrids,
- when you replace the hard drive or any other assembly,
- when the oscilloscope's operating temperature (after the 30 minute warm-up period) is more than ±5 °C different from that of the last calibration.

Internal or Self Calibration

NOTE **Calibration time: It takes approximately 1 hour to run the self calibration on the Oscilloscope, including the time required to change cables from Channel to Channel.**

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Keysight oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:
   - *a* Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.
   - *b* Plug in the power cord.
   - *c* Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.
   - *d* Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:
   - *a* Locate the BNC shorting cap.
   - *b* Locate the calibration cable.
   - *c* Locate the two Keysight precision SMA/BNC adapters.
   - *d* Attach one SMA adapter to the other end of the calibration cable — hand tighten snugly.
   - *e* Attach another SMA adapter to the other end of the calibration cable — hand tighten snugly.

3 From the Infiniium Oscilloscope's main menu, click **Utilities>Calibration...**.

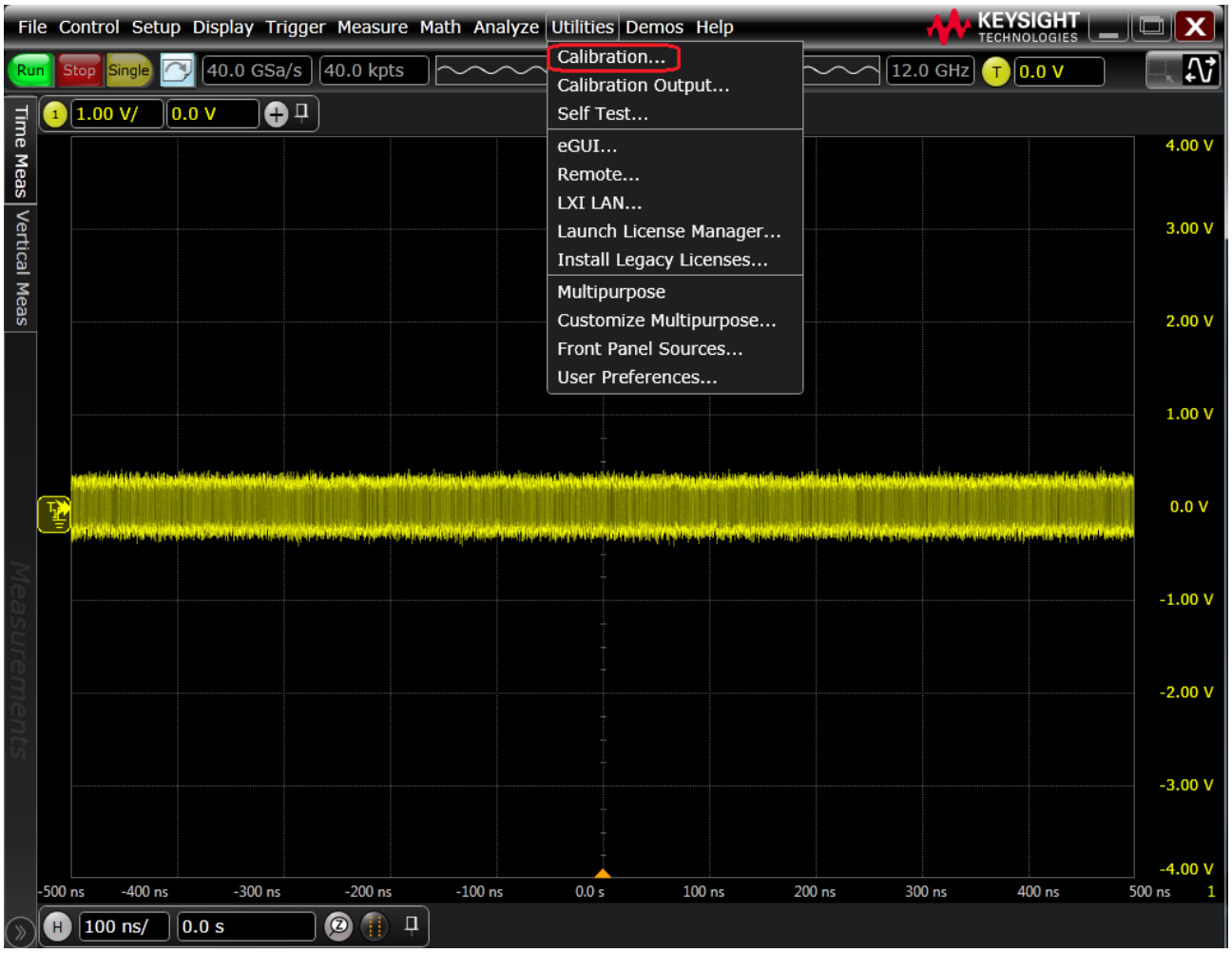


Figure 95 Accessing Calibration dialog on the Oscilloscope

The **Calibration** dialog appears.

4 To start the calibration process:

a Clear the **Cal Memory Protect** checkbox.

You cannot run self calibration if this box is checked. See Figure 96.

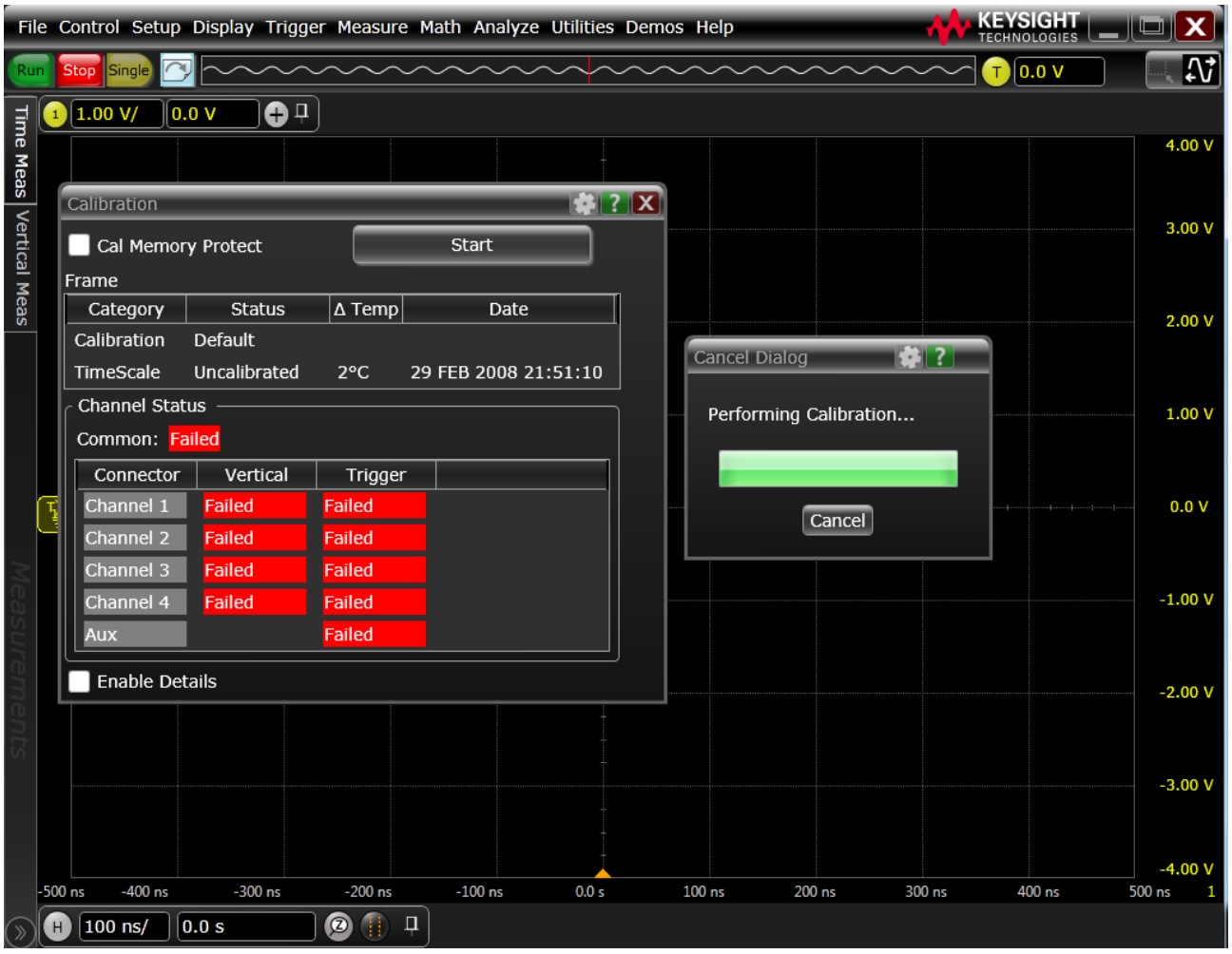


Figure 96 Clearing **Cal Memory Protect** and Starting Calibration

b Click **Start** to begin calibration.

c Follow the on-screen instructions.

d During the calibration of any Oscilloscope Channel, if the oscilloscope prompts you to perform a Time Scale Calibration, select **Standard Cal and Default Time Scale** in the **Calibration Options** dialog.

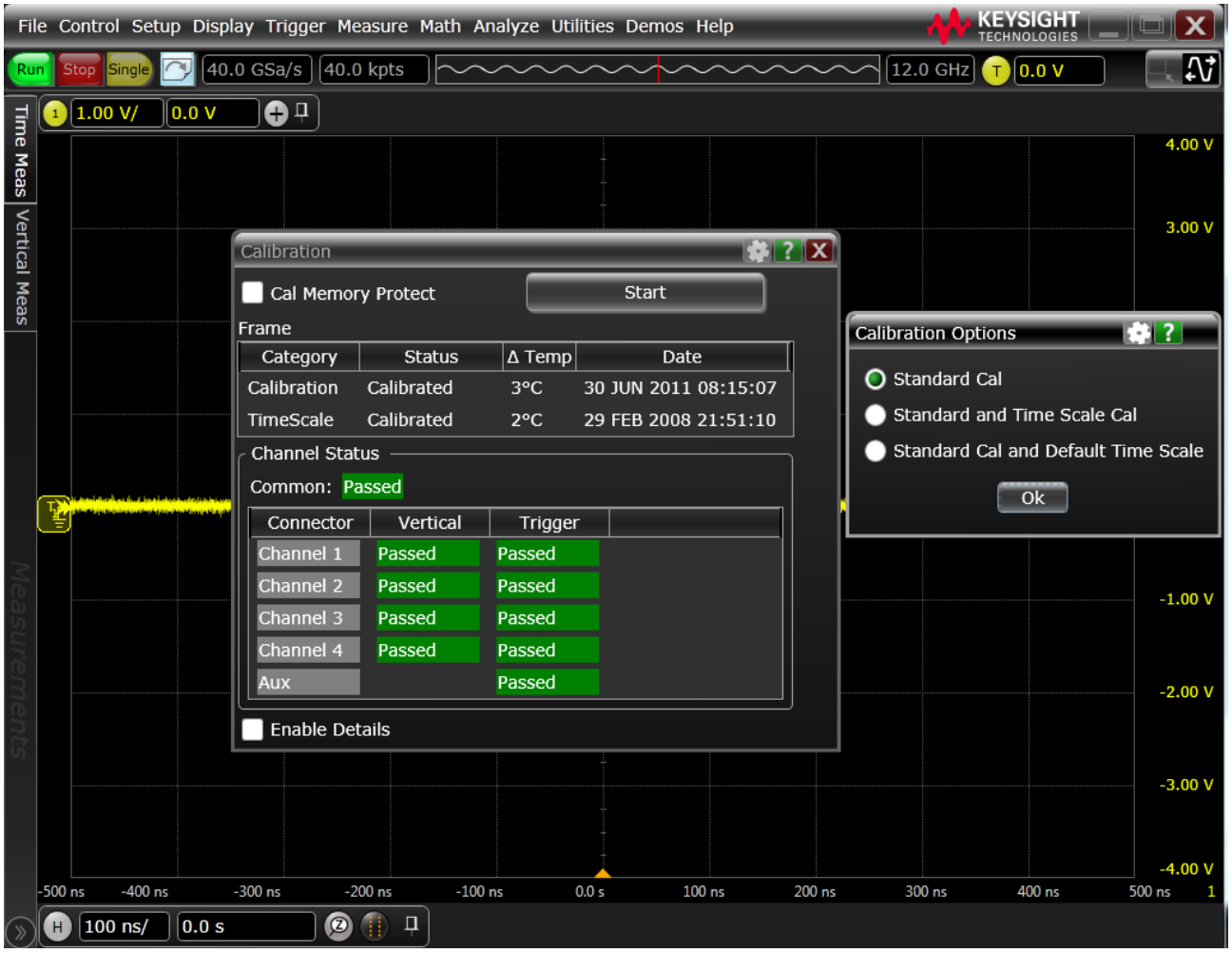


Figure 97 Selecting options from the **Calibration Options** dialog

The options under the **Calibration Options** dialog are:

- **Standard Calibration**—Oscilloscope does not perform time scale calibration and uses calibration factors from the previous time scale calibration and the reference signal is not required. The rest of the calibration procedure continues.
- **Standard and Time Scale Cal**—Oscilloscope performs time scale calibration. You must connect a reference signal to the Oscilloscope Channel, after ensuring that the reference signal meets the following specifications. Failure to meet these specifications result in an inaccurate calibration.

- **Standard Cal and Default Time Scale**—Oscilloscope uses the default time scale calibration factors and does not require the 10 MHz reference signal. The rest of the calibration procedure continues.

e Disconnect everything from all inputs and Aux Out.

f Connect the calibration cable from Aux Out to a specific Channel.

g Connect the calibration cable from Aux Out to each of the Channel inputs as requested.

h Connect the 50 **Ω** BNC cable from the Aux Out to the Aux Trig on the front panel of the Oscilloscope.

i A Passed/Failed indication is displayed for each calibration section. If any section fails, check the calibration cables and run the Oscilloscope **Self Test...** in the **Utilities...** menu.

j After the calibration procedure is completed, click **Close**.

NOTE These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities>Calibration** menu.

Probe Calibration and De-skew

Along with calibrating the Infiniium Oscilloscope, it is a good practice to calibrate and de-skew the probes, before you start running the automated tests.

Required Equipment for Probe Calibration

Before performing the compliance tests, calibrate the probes. Calibration of the solder-in probe heads consists of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adapter
- Deskew fixture
- 50 Ω SMA terminator

SMA Probe Head Attenuation/Offset Calibration

Perform the following steps

1. Connect BNC (male) to SMA (male) adapter to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the 50 Ω SMA terminator to the connector farthest from the yellow pincher.
3. Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
4. Connect the probe to an oscilloscope channel.
5. To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
6. Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
7. Release the yellow pincher.

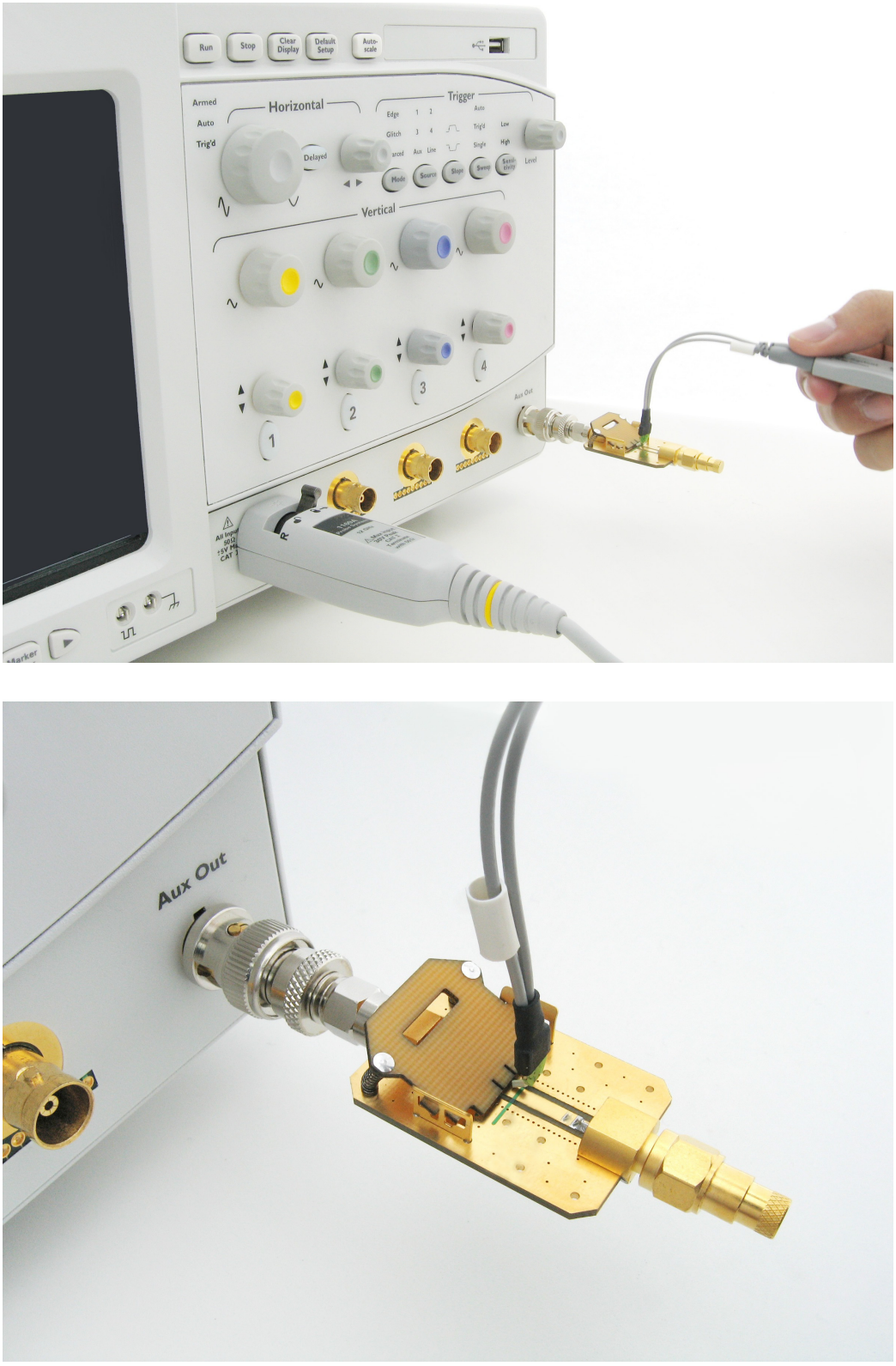


Figure 98 Example of Solder-in Probe Head Calibration Connection

8 To verify the connection, press the autoscale button on the front panel of the Infiniium Oscilloscope.

9 Set the volts per division to 100 mV/div.

10 Set the horizontal scale to 1.00 ns/div.

11 Set the horizontal position to approximately 3ns. A waveform similar to the one displayed in Figure 99 must appear.

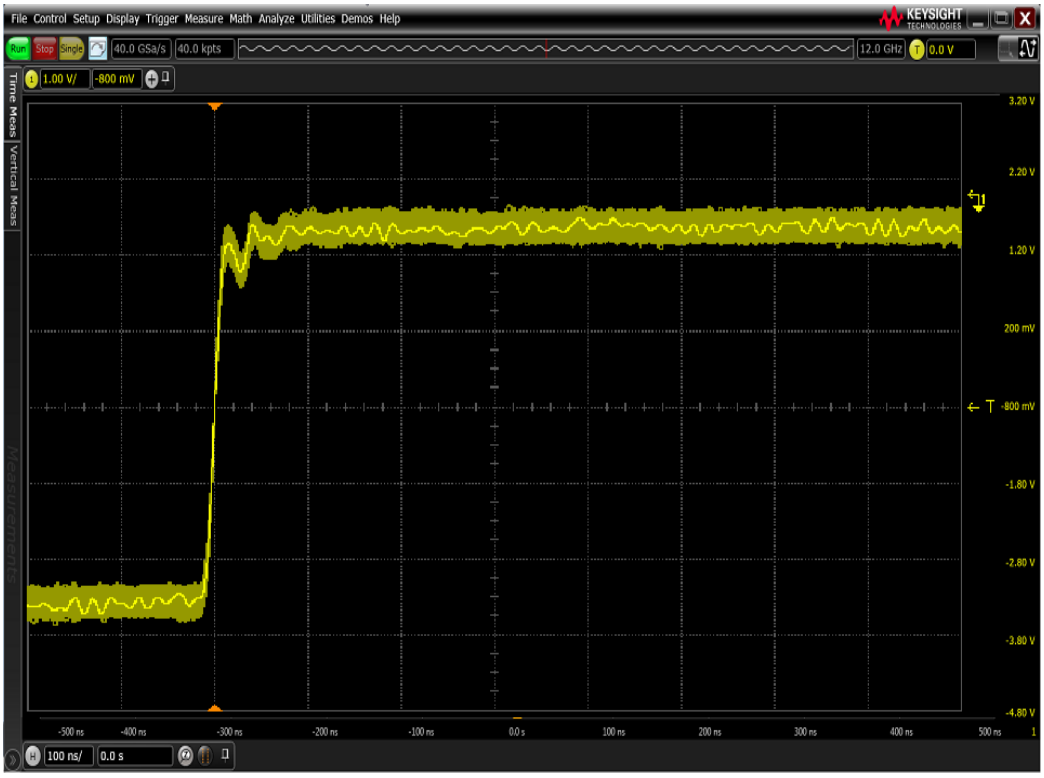


Figure 99 Example of a waveform when the probe connection is good

If a waveform similar to that shown in Figure 100 appears, it indicates that there is a bad connection and you must check all your probe connections.

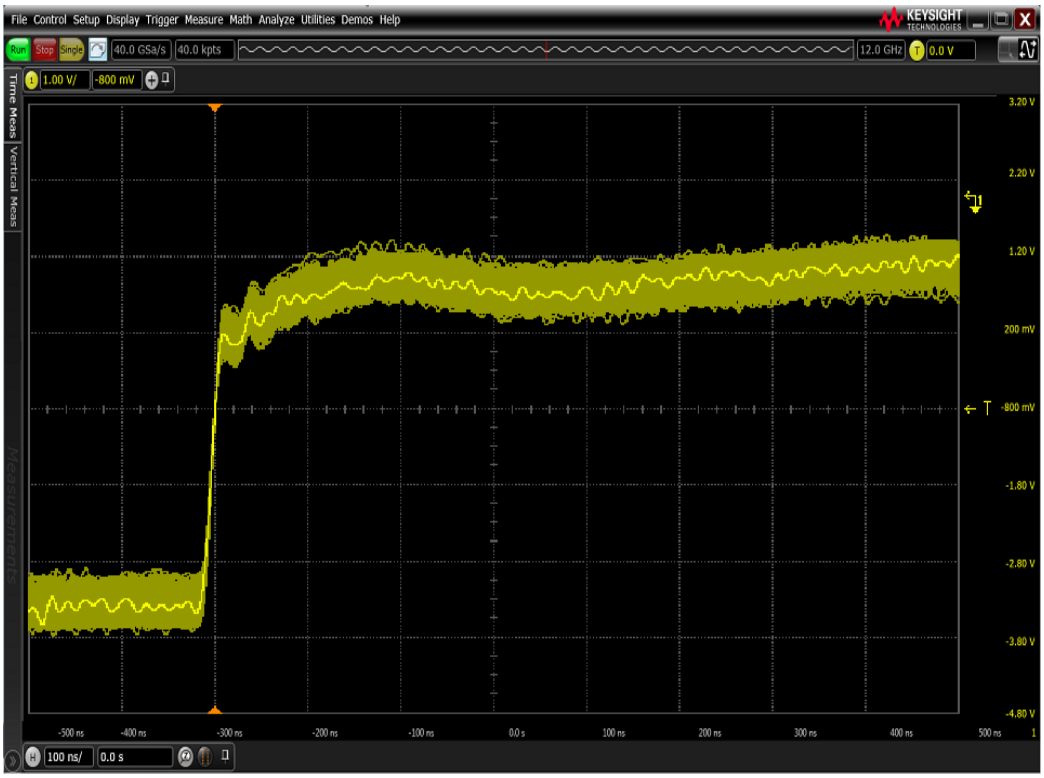
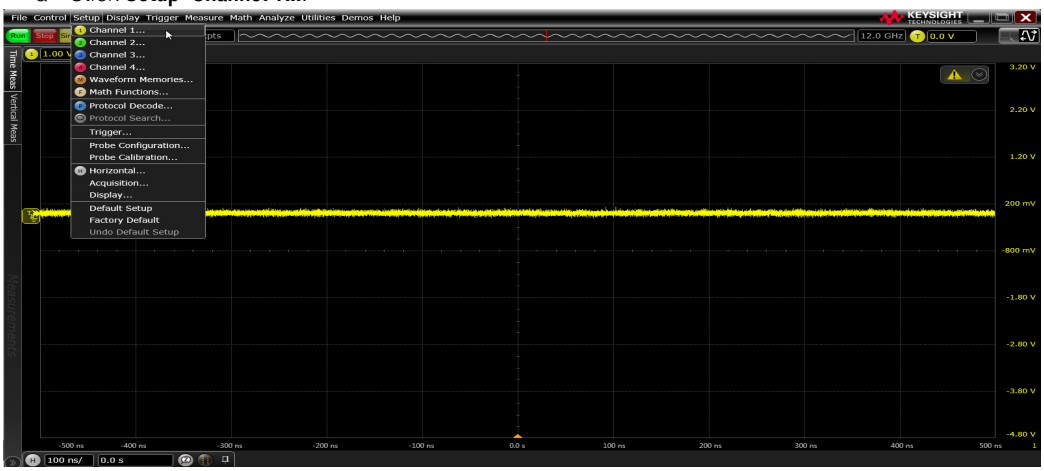


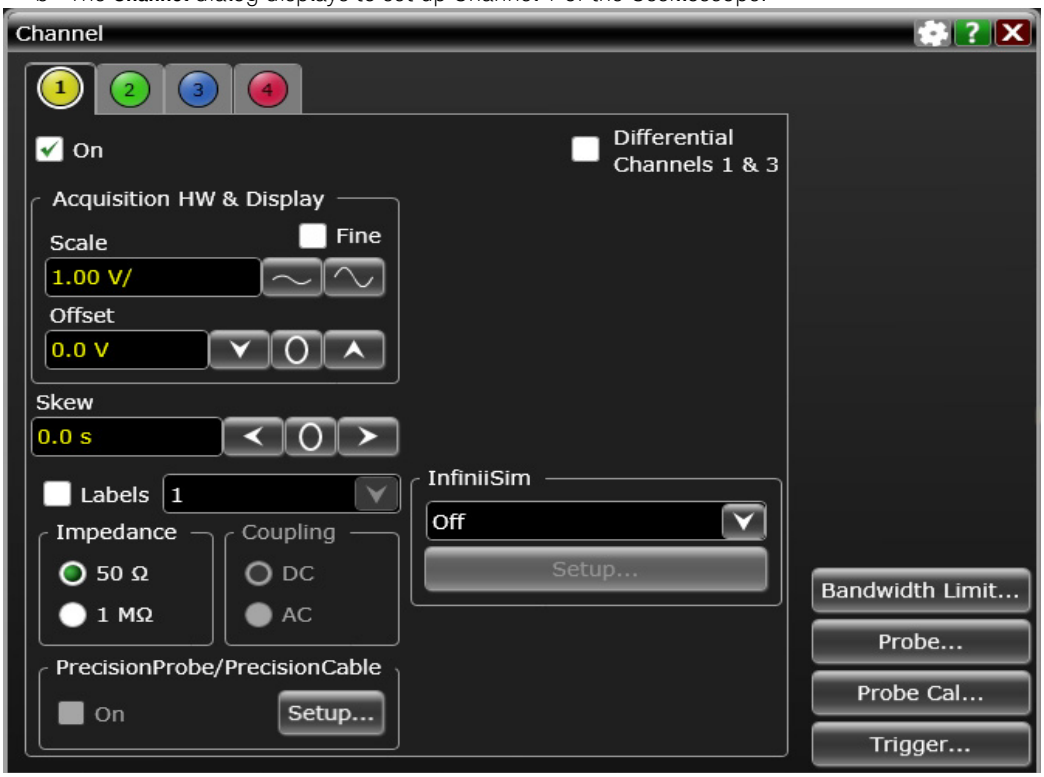
Figure 100 Example of a waveform when the probe connection is bad

12 On the Infiniium Oscilloscope,

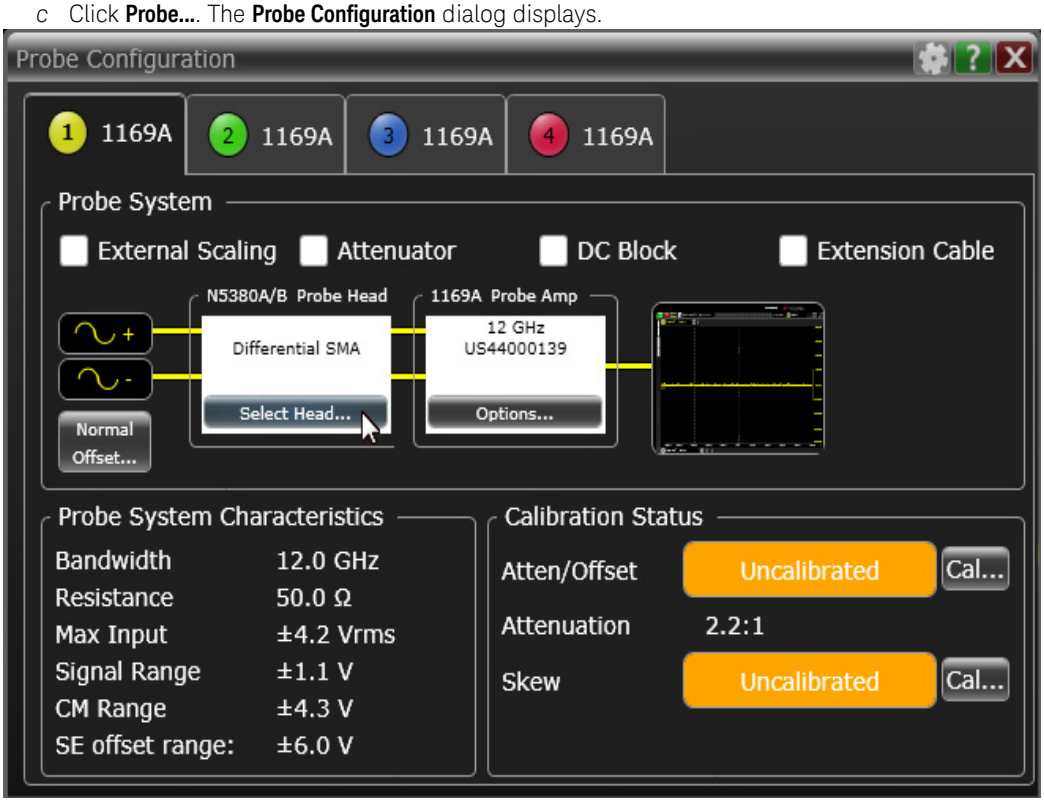
a Click **Setup>Channel 1...**.



b The **Channel** dialog displays to set up Channel 1 of the Oscilloscope.



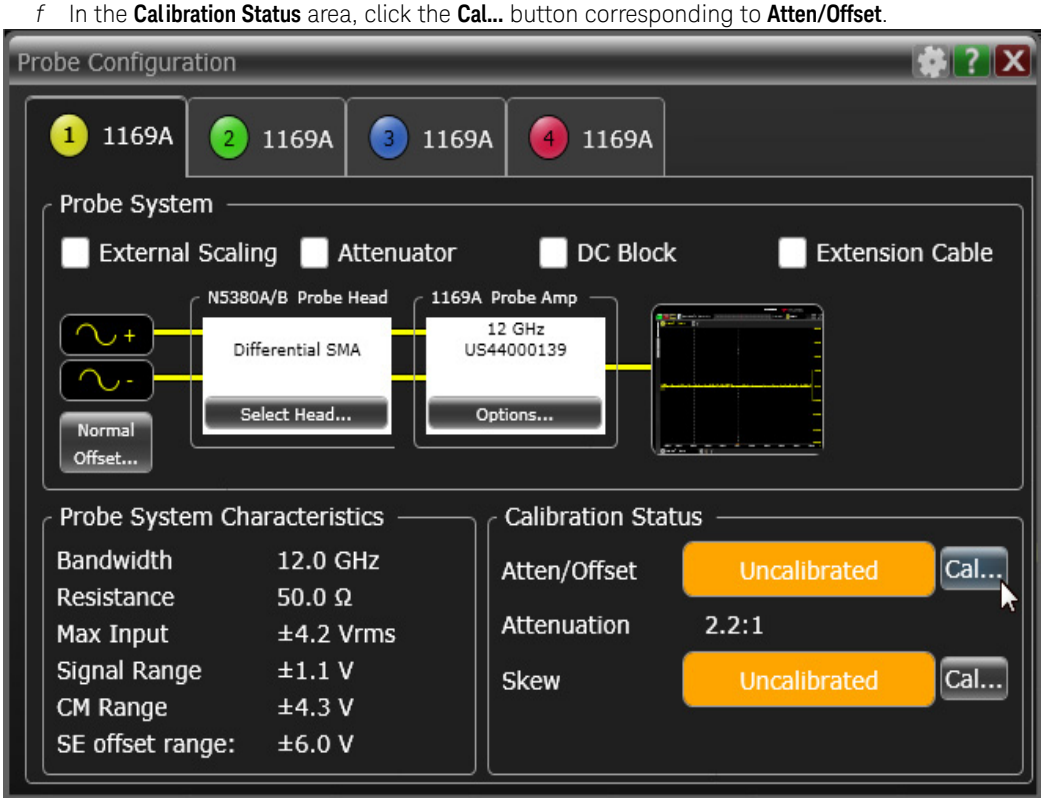
c Click **Probe...**. The **Probe Configuration** dialog displays.



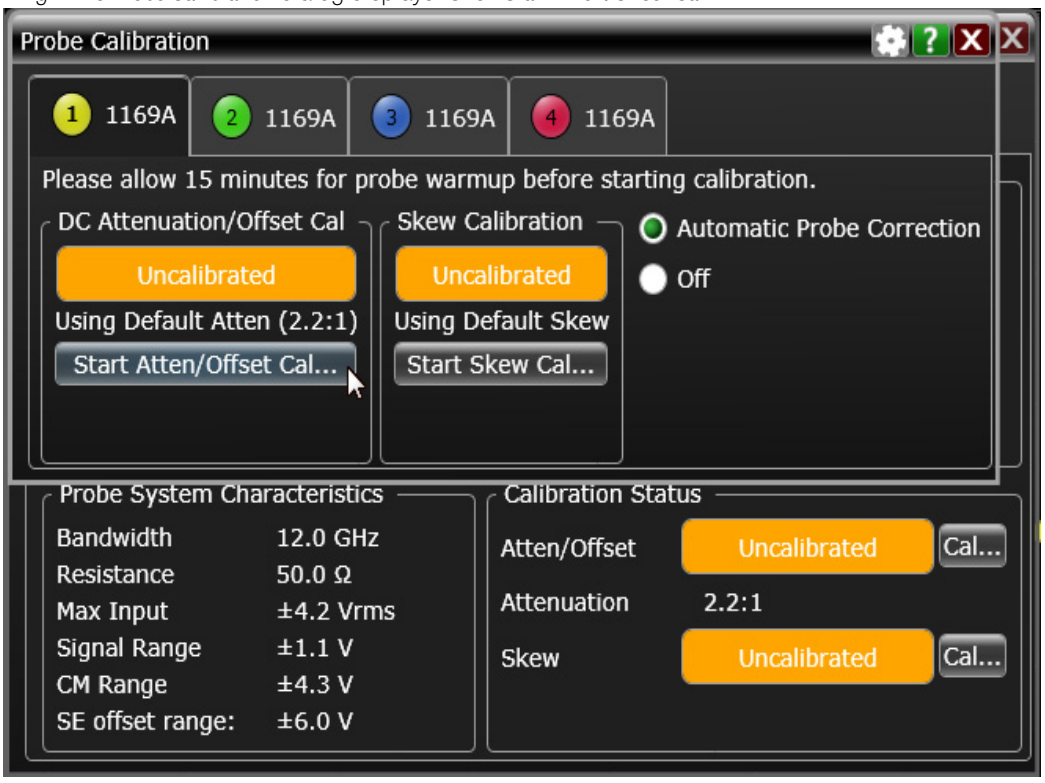
d In the **Differential SMA** block, click the **Select Head...** button.

e Select **N5380A/B** from the list.

f In the **Calibration Status** area, click the **Cal...** button corresponding to **Atten/Offset**.



g The **Probe Calibration** dialog displays. Click **Start Atten/Offset Cal...**.



h The Calibration wizard displays. Follow the on-screen instructions. At the end of the Atten/Offset Calibration, perform the Skew calibration for the SMA Probe Head.

SMA Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. After the Atten/Offset Calibration is done, perform the following steps for skew calibration:

1 On the **Probe Calibration** dialog, click **Start Skew Cal...**.

2 The Calibration wizard displays. Follow the on-screen instructions.

Differential SMA Probe Head Atten/Offset Calibration

Perform the following steps

1 Ensure that a probe, attached to an SMA Probe Head is connected to Channel 1 of the Oscilloscope.

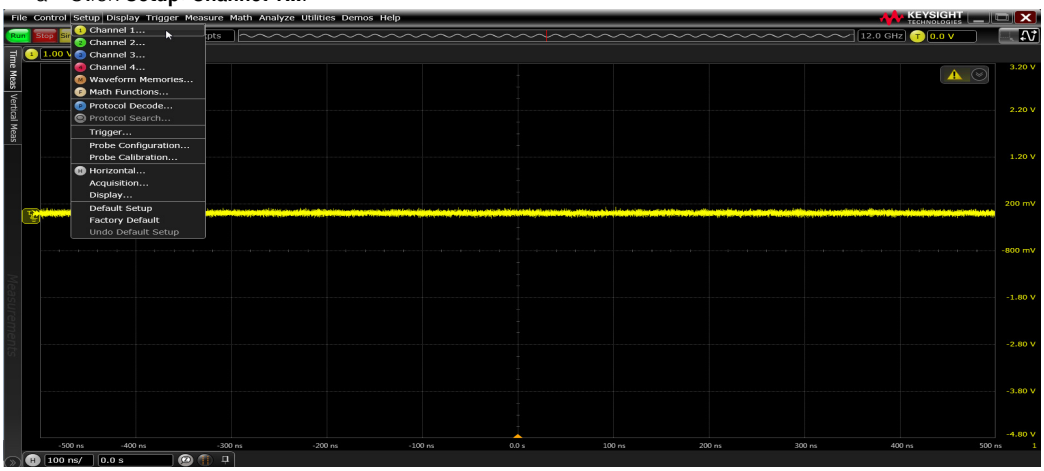
2 Install the 80 Ω resistors into the SMA Probe Head. These resistors are required only for probe calibration and de-skew.

3 Connect the De-skew fixture to AUX Out.

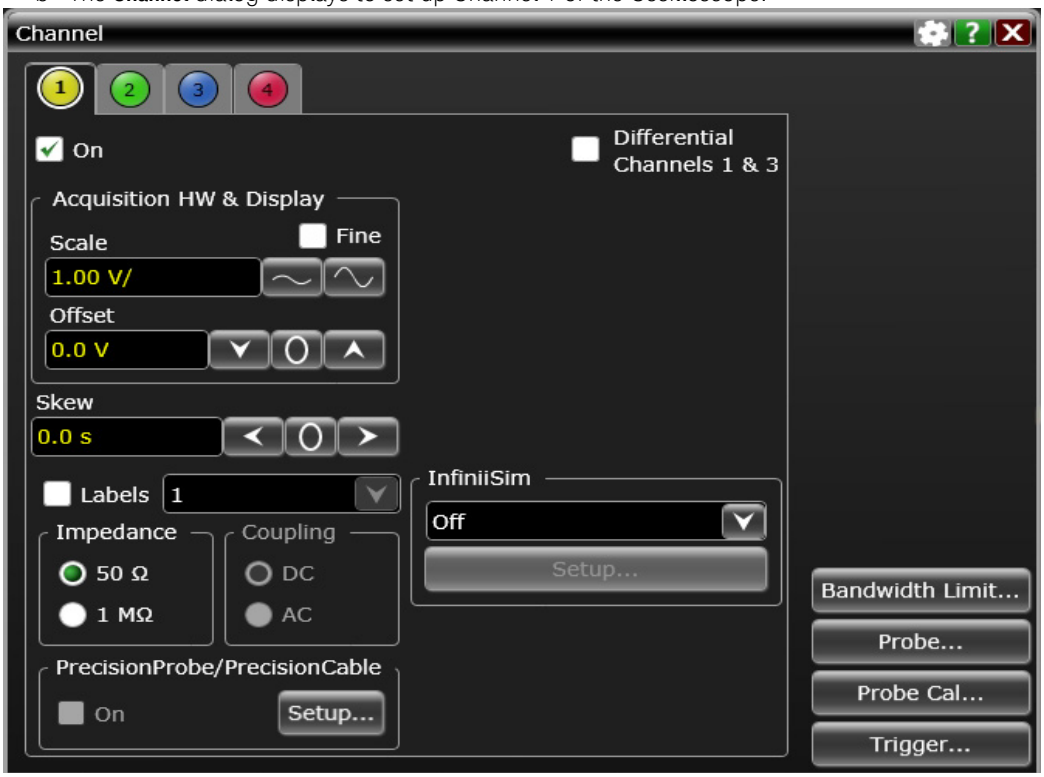
4 Clip the resistors on the De-Skew fixture.

5 On the Infiniium Oscilloscope,

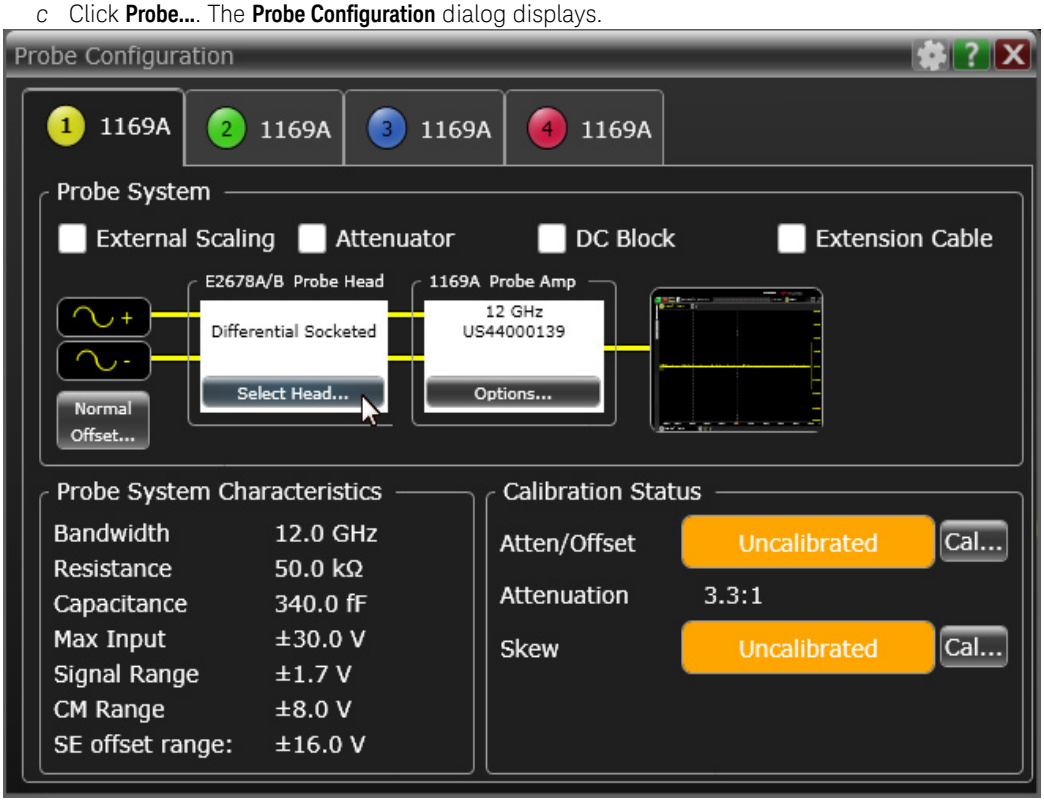
a Click **Setup>Channel 1...**.



b The **Channel** dialog displays to set up Channel 1 of the Oscilloscope.



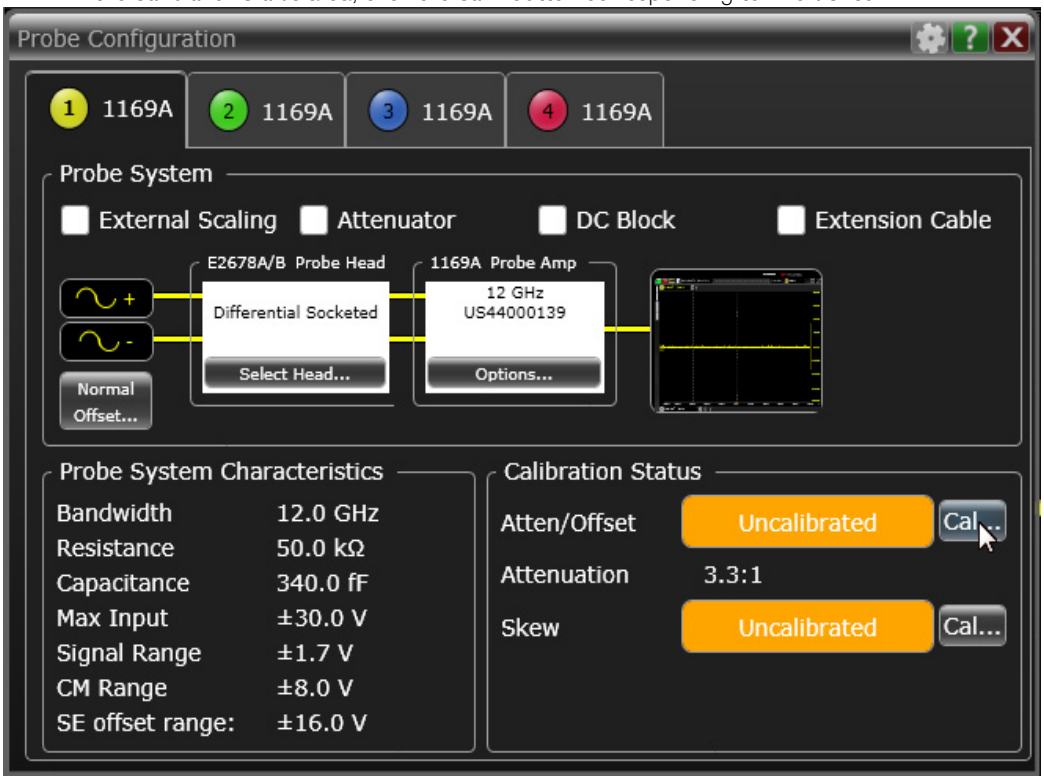
c Click **Probe...**. The **Probe Configuration** dialog displays.



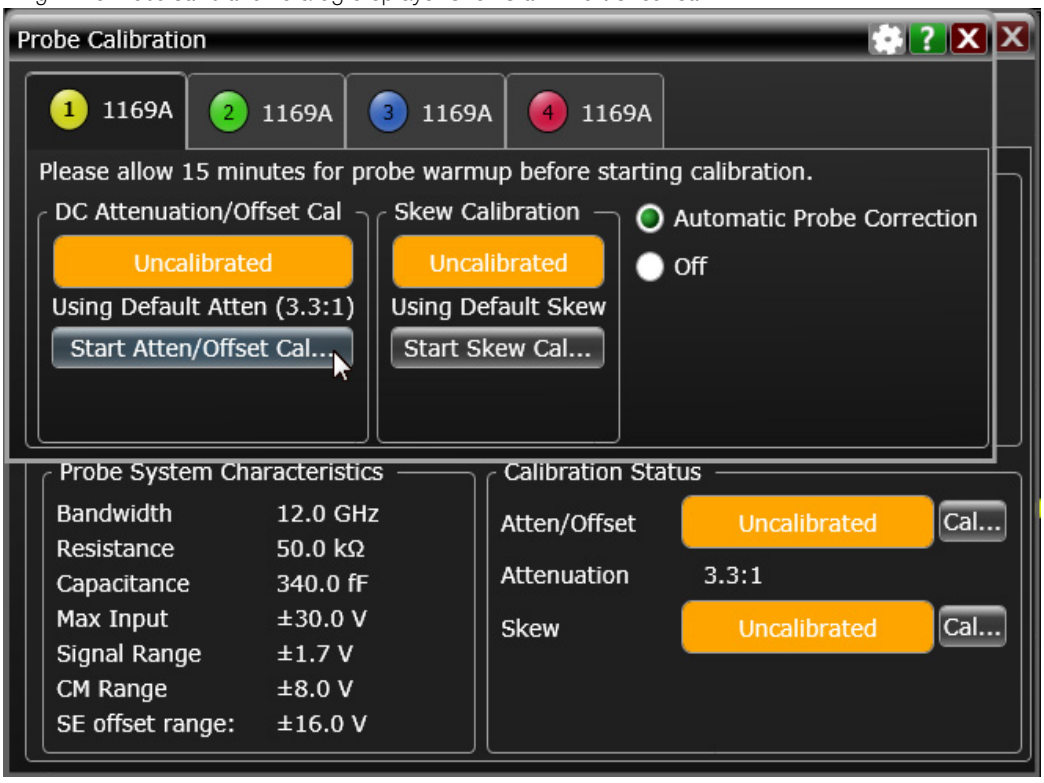
d In the **Differential Socketed** block, click the **Select Head...** button.

e Select **E2678A/B** from the list.

f In the **Calibration Status** area, click the **Cal...** button corresponding to **Atten/Offset**.



g The **Probe Calibration** dialog displays. Click **Start Atten/Offset Cal...**.

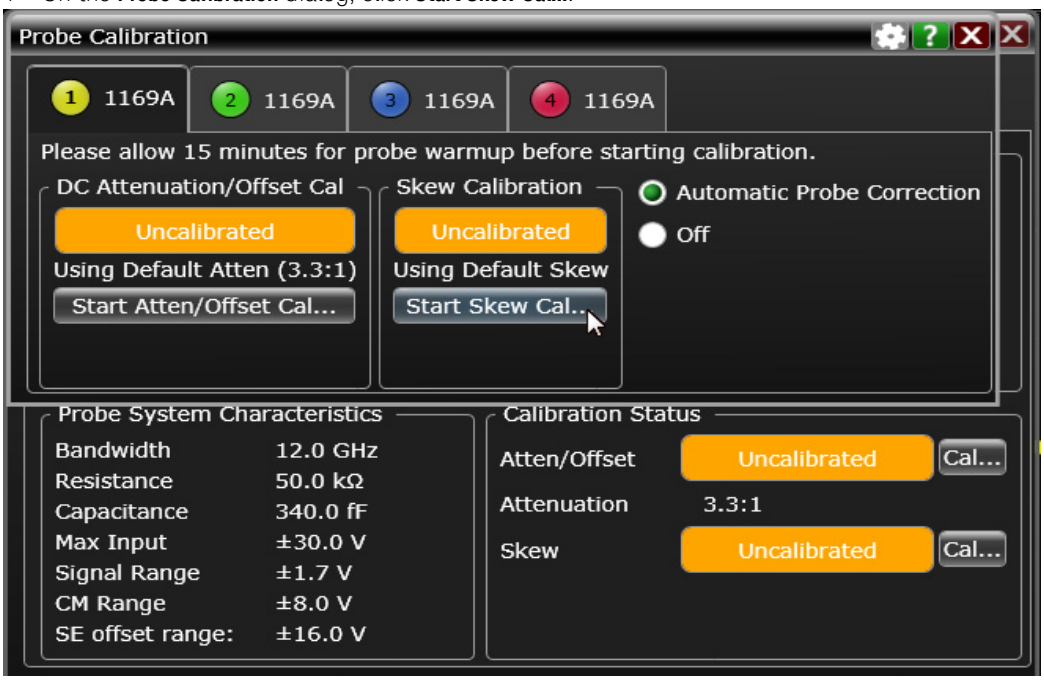


h The Calibration wizard displays. Follow the on-screen instructions. At the end of the Atten/Offset Calibration, perform the Skew calibration for the Differential SMA Probe Head.

Differential SMA Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. After the Atten/Offset Calibration is done, perform the following steps for skew calibration:

1 On the **Probe Calibration** dialog, click **Start Skew Cal...**.



2 The Calibration wizard displays. Follow the on-screen instructions.

For more information on connecting probes to the Infiniium Oscilloscope, refer to the De-skew and Calibration manual. This manual comes together with the E2655A/B/C Probe De-skew and Performance Verification Kit.

NOTE Each probe is calibrated to the Oscilloscope Channel to which it is connected. Do not switch probes between Channels or other Oscilloscopes, else it becomes necessary to calibrate them again. One of the best practices is to label the probes with the Channel number on which they are calibrated.

7 InfiniiMax Probing

This section describes the recommended InfiniiMax Probes used with Keysight Infiniium Oscilloscopes.

Figure 101 1134A InfiniiMax Probe Amplifier

Keysight recommends 116xA or 113xA probe amplifiers, which range from 3.5 GHz to 12 GHz.

Keysight also recommends the E2677A differential solder-in probe head. Other probe head options include N5381A InfiniiMax II 12 GHz differential solder-in probe head, N5425A InfiniiMax ZIF probe head and N5426A ZIF Tips.

Figure 102 E2677A / N5381A Differential Solder-in Probe Head

Table 12 Probe Head Characteristics (with 1134A probe amplifier)

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential Solder-in	E2677A	7 GHz, 0.27 pF, 50 kOhm	7 GHz, 0.44 pF, 25 kOhm

Used with 1168A or 1169A probe amplifier, the E2677A differential solder-in probe head provides 10 GHz and 12 GHz bandwidth respectively.

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